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A Proposed Conceptual Architecture for Time-Sensitive Software-Systems

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Research Question:

«Time-Sensitive Software» (Lee et al., 2023)

Abstract

Many mission-critical systems today have stringent timing requirements. Especially for cyber-physical systems that directly interact with real-world entities, violating correct timing may cause accidents, damage, or endanger life, property, or the environment. To ensure the timely execution of time-sensitive software, a suitable system architecture is essential. This paper proposes a novel conceptual system architecture based on well-established technologies, including transition systems, process algebras, Petri Nets, and time-triggered communications. This architecture for time-sensitive software execution is described as a conceptual model backed by an extensive list of references and opens up several additional research topics. This paper focuses on the conceptual level and defers implementation issues to further research and subsequent publications.

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Time in Computing

Time is a fascinating concept. Much has been thought and written about the physics of time (e.g., Muller, 2016), the philosophy of time (e.g., Power, 2021), the measurement of time (e.g., Struthers, 2024), and the history of time (e.g., Hawking, 2015). In computing, time has precise meanings (Furia, 2012 / Buttazzo, 2024), such as:

(1) The time elapsed between an event and the completion of the correct response (Latency);
(2) The maximum time guaranteed for a program to execute (Worst case execution time, WCET);
(3) The maximum time allowed for the execution of a process or a function (Before a time-out);
(4) The maximum time for a process to wait for an event, a response, or a message (Synchronization);
(5) The time interval between measurement values received from a sensor (Input sampling rate);
(6) The time interval between outputs to an actuator (Output sampling rate);
(7) The trigger times to start a process (Either absolute from UCT or relative to another event or process);
(8) Relative timing: Before, not before, after (For events, messages, actions, process start, etc.);
(9) … and other timing requirements or timing relationships.

Timing is a serious specification responsibility. In cyber-physical systems, strict adherence to correct timing requirements is a decisive safety property. Therefore, time-sensitive software is crucial for safety-critical cyber-physical systems!

State of the Art

The work on reference architectures for cyber-physical systems (e.g., Nakagawa et al., 2023) is not new. Several such architectures have been proposed and are well documented, e.g., generic architectures, such as: CPS 5 Components Architecture (Ahmadi et al., 2021), 8C architecture (Sony, 2020), NIST Framework for Cyber-Physical Systems (Griffor et al., 2017 / NIST, 2017). Or domain-specific architectures, such as: AUTOSAR (https://www.autosar.org/ Rajeev et al., 2012), IMA (Integrated Modular Avionics

Architecture, Gaska et al., 2015). Some architecture-centric standards, such as ISO 26262 (see, e.g., Debouk, 2019) and IEC 61499 (see, e.g., Thramboulidis, 2012; Yoong et al., 2013, 2016), are highly useful. However, these works treat timing as a *quality attribute* (= measurable or testable characteristics of a system, such as availability, reliability, usability, or scalability) and not as a *correctness property* of the system (= formal requirement that defines and assures the system's expected behavior), (Lee et al., 2023).

A different approach to handling time is the use of temporal logic. Many types of temporal logic systems exist (e.g., 16 of them are explained in Bellini et al., 2000). Temporal logic extends classical logic by defining temporal operators, allowing engineers to model and reason about the behavior of systems over time. Using temporal logic is a powerful methodology in software engineering, applicable to the specification, verification, and design of programs, algorithms, and databases (e.g., Bolc et al., 2019; Furia et al., 2012; Kröger et al., 2008). Temporal logic expresses timing well but cannot define and express the system architecture (Structure, relationships, attributes).

A different, generic, layered architecture has been proposed by Ungureanu et al. (2017). Their proposal utilizes different constructs, including the tagged signal model, the functional programming paradigm, and algorithmic skeletons. An additional framework is developed by Abdellatif et al. (2010) and Buckl et al. (2010), focusing on timing and safety.

The progress of this paper is a *conceptual* architecture with explicit, formalized, verifiable timing at all levels of the architecture and all steps of the lifecycle of the CPS:

I. Elevating timing from a *quality attribute* (= measurable or testable characteristics of a system, such as availability, reliability, usability, or scalability) to a *correctness property* of the system (= formal requirement that defines and assures the system's expected behavior);
II. Proposing a layered architecture that respects the proven, well-documented architecture principles, such as layering, partitioning, modularization, loose coupling, separation of concerns, etc. (Furrer, 2019 / Furrer, 2022);
III. Combines accepted constructs for timing definition, verification, and implementation (Process algebra, transition systems, Petri Nets, Time-Triggered Communications).

Introduction and Context

The context for time-sensitive software is shown in Figure 1. It consists of 6 elements:

1. The functional processes: These processes specify the functionality of the system. Note that the term is mainly used for business processes, but technical functionality is also represented as a (functional) process. The symbol τ represents the timing requirements of the process. Note that complete and correct error- and exception-handling is an indispensable and integral part of the processes (e.g., Öztemür, 2015);
2. The components (programs) implementing the functionality;
3. The execution platforms (processors, memory, communications, databases, etc.): Note that most of today's cyber-physical systems are distributed systems, i.e., they have more than one execution platform. Such systems are referred to as systems-of-systems (SoS). The different execution platforms communicate with each other – they are linked by one or several communication channels;
4. The interprocess-communication: The processes exchange information and flow control (such as synchronization, checkpoints);
5. Mechanism for the process orchestration. Start, stop, or interrupt processes, e.g., following an event, a message, a timing, or a schedule;
6. The connection to the real world: Sensors to read information, and actuators to control the physical world.

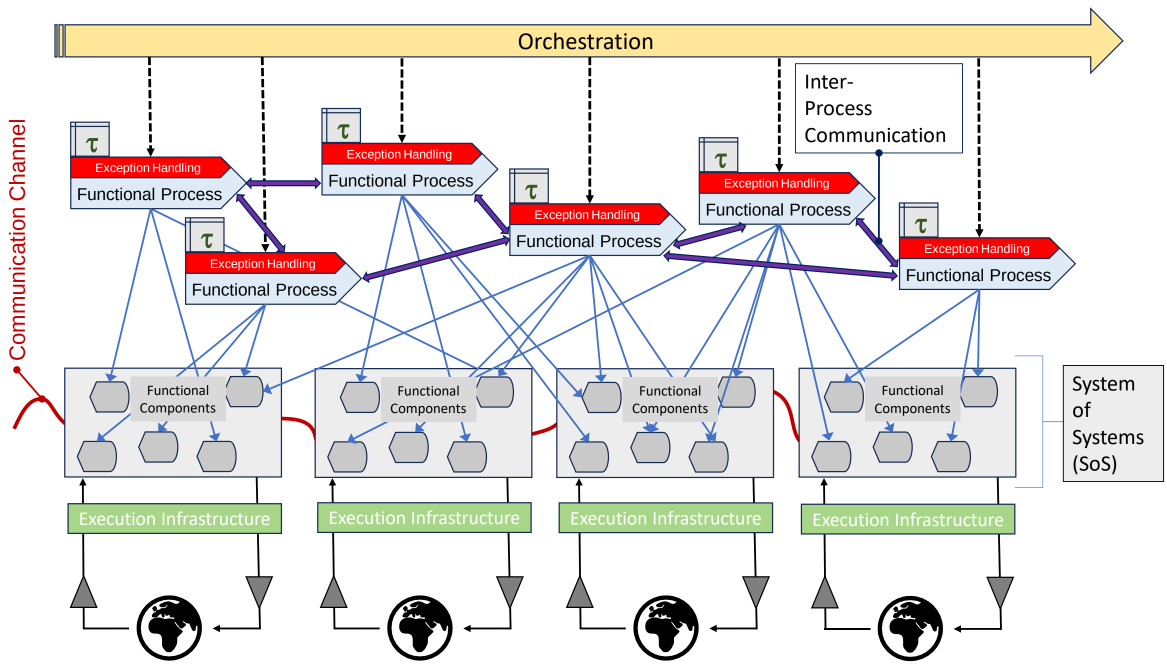
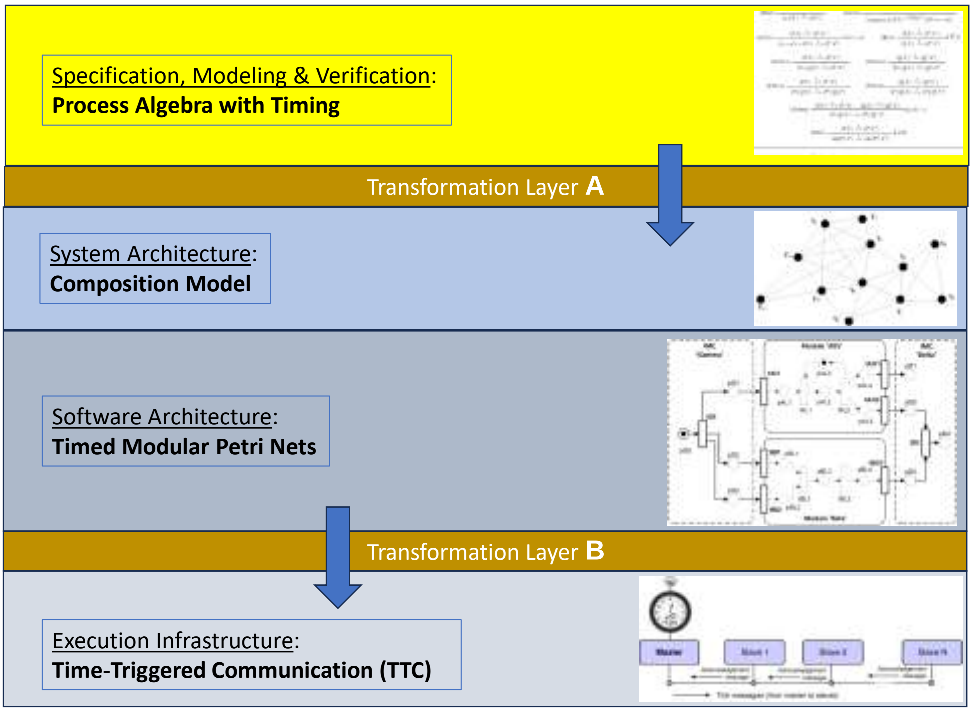


Figure 1: Context for Time-Sensitive Software

Layered Architecture Proposal

Context: All development and evolution mechanisms for time-sensitive software – from specification to operation – must have the proper constructs for correctly handling time. Unfortunately, most of today's methodologies and tools lack a consistent and verifiable handling of time – and are thus only of limited use for developing and verifying time-sensitive software.

Figure 2 is an attempt at a conceptual end-to-end architecture for time-sensitive software. Please note that this first sketch is a conceptual proposal and leaves open points for future research.



https://www.researchgate.net/figure/Simple-architecture-of-time-triggered-shared-clock-scheduler_fig1_308611848

Figure 2: Layered Architecture Proposal

Figure 2 proposes six architecture layers, each one with formal constructs to handle time explicitly:

I. *The specification, modeling, and verification layer* (Top layer): For this layer, a process algebra is used. Process algebra is a formal calculus for specifying, modeling, and verifying transition processes (DeNicola, 2011/Aldini et al., 2009/ Fokkink, 1999/Chao, 2015). Some process algebras include the formal constructs for timing (e.g., Baeten, 2001 /Baeten, 2002 / Wang, 2002 / Wolf, 2002);

II. *The system architecture layer*: Describes the parts (= components), their composition (= structure), and their relationships (= interactions). As a composition model, "Petri Nets for Modeling of Large Discrete Systems" (Davidrajuh, 2021) is utilized;

III. *The software architecture layer*: As the component model providing the functionality, "Petri Modules" and "Inter-modular connectors" (Davidrajuh, 2021) are selected. The Petri modules are enriched with timing constructs (Popova-Zeugmann, 2016 / Liu, 2022);

IV. *The execution infrastructure layer*: All software runs on the execution infrastructure layer. This layer encompasses all hardware, software systems, and communication elements. Again, an execution infrastructure that is time-aware, i.e., can provide execution timing guarantees, must be provided. The infrastructure of choice is the "Time-Triggered Communications" (Obermaisser et al., 2012 /Kopetz, 2022/Kopetz et al., 2003/Maier et al., 2002/ Rushby, 2005/Buttazzo, 2023);

V. In addition, two *transformation layers* are required. Transformation Layer A translates the verified specification model into the Petri Net specifications. Note that the system architecture (Petri Net structure) is designed before the transformation A. Transformation layer B maps the timed functionality of the Petri Nets to the TTA schedule, i.e., to the execution infrastructure.

Concurrency and Latency

The two most challenging topics in implementing time-critical CPS are *concurrency* (e.g., Gorrieri et al., 2015) and *latency* (e.g., Kopetz et al., 2022). In a modern CPS, many applications share common resources, such as CPUs, memory, external storage, and communications channels, i.e., parallel access to shared resources (Figure 3). This concurrency may result in one application or process influencing the timing of another application or process, sometimes adversarially, such that timing requirements may be violated, such as response times prolongated! If concurrency is not handled correctly, non-determinism can occur – delivering different results from a program run because of interference by concurrency (Gorrieri et al., 2015).

The second topic is latency (Figure 3): In a classical architecture implementation, there are many sources of latency: Operating system functions, scheduling, communications delays, shared memory access retardation, queuing, etc. Some of these delays may be unpredictable and can behave statistically. For dependable time-sensitive software, concurrency and latency must be identified, quantified, and adequately managed. The proposed architecture in Figure 2 is designed to strongly support this objective.

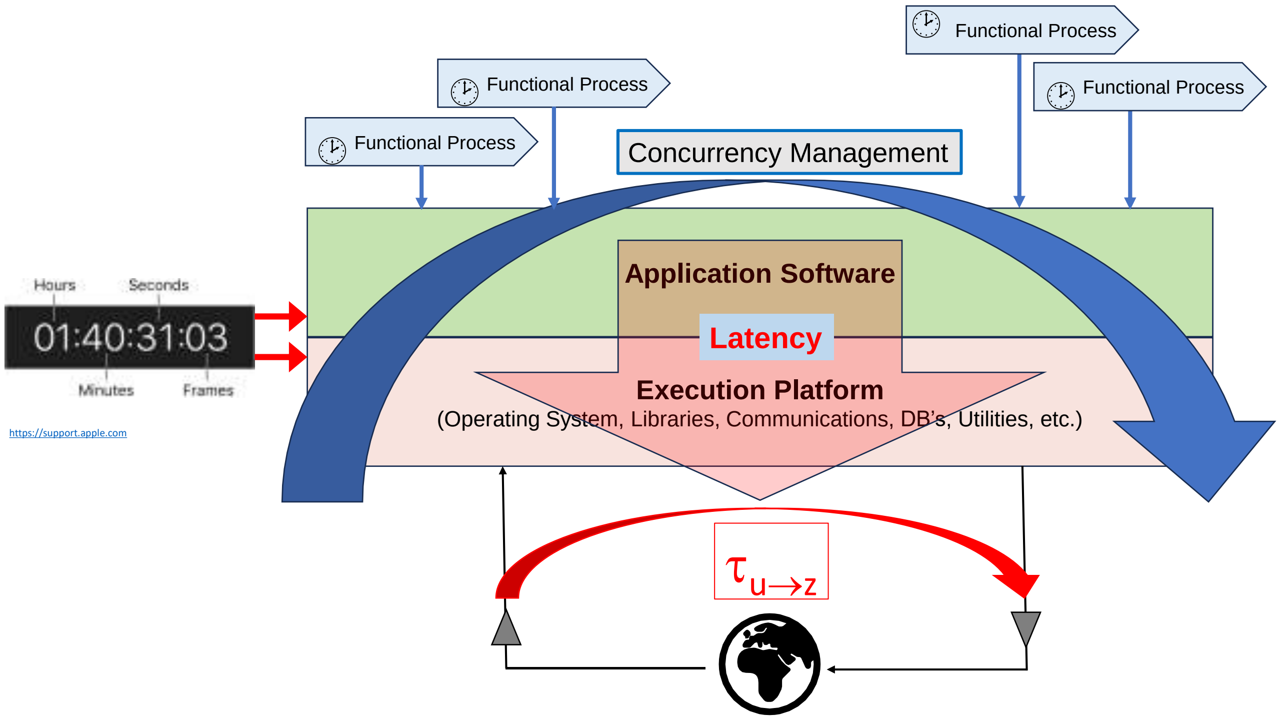


Figure 3: Concurrency and Latency in a Computing System

Process Algebra

Context: For the specification, verification, and modeling of the time-aware functional processes in the system (Top level layer of Figure 2), the methodology of Process Algebras with Time is chosen (e.g., Baeten, 2001/Baeten, 2002 / Wang, 2002). Process algebras are formalisms for specifying interactions (synchronization, flow control, semaphores, etc.) between concurrent processes. Modern process algebras evolved from the idea of formalizing communicating processes. The seminal contribution is the paper "A Calculus of Communicating Systems (CSS)" (Milner, 1980). In the following years, several new Process Algebras were developed (e.g., Baeten, 2005/Bergstra, 1984/Hoare, 1985). The early process algebras had no explicit and formal notion of timing. Timing was introduced later (e.g., Nicollin, 1991). Today, process algebras with fully formalized timing exist (e.g., Baeten, 2001 /Baeten, 2002 / Wang, 2002). A process algebra defines a set of operators for the interaction of concurrent processes. A process algebra with time has additional operators for formally handling time.

Many process algebras with rich literature are in use today (e.g., Aceto, 2003). So far, no favorite, widely accepted, and used process algebra exists. Process algebras are selected for the task at hand. For the widespread use of process algebras in industry, standardization by an industry body would be highly beneficial. A first attempt is the ISO standardization of a process algebra for communication protocols (Bolognesi et al., 1968 / ISO, 2001).

Transition Processes

Context: Process algebras require modeling the functionality of processes as transition systems (e.g., Demri et al., 2016; Gorrieri et al., 2015).

Transition systems have states. An action triggers the transition from one state to another. States and actions include explicit timing requirements in their specifications (Figure 4a, the symbol 🕑 represents the timing). The theory of state machines is well-known and provides sufficient formality (e.g., Börger et al., 2013).

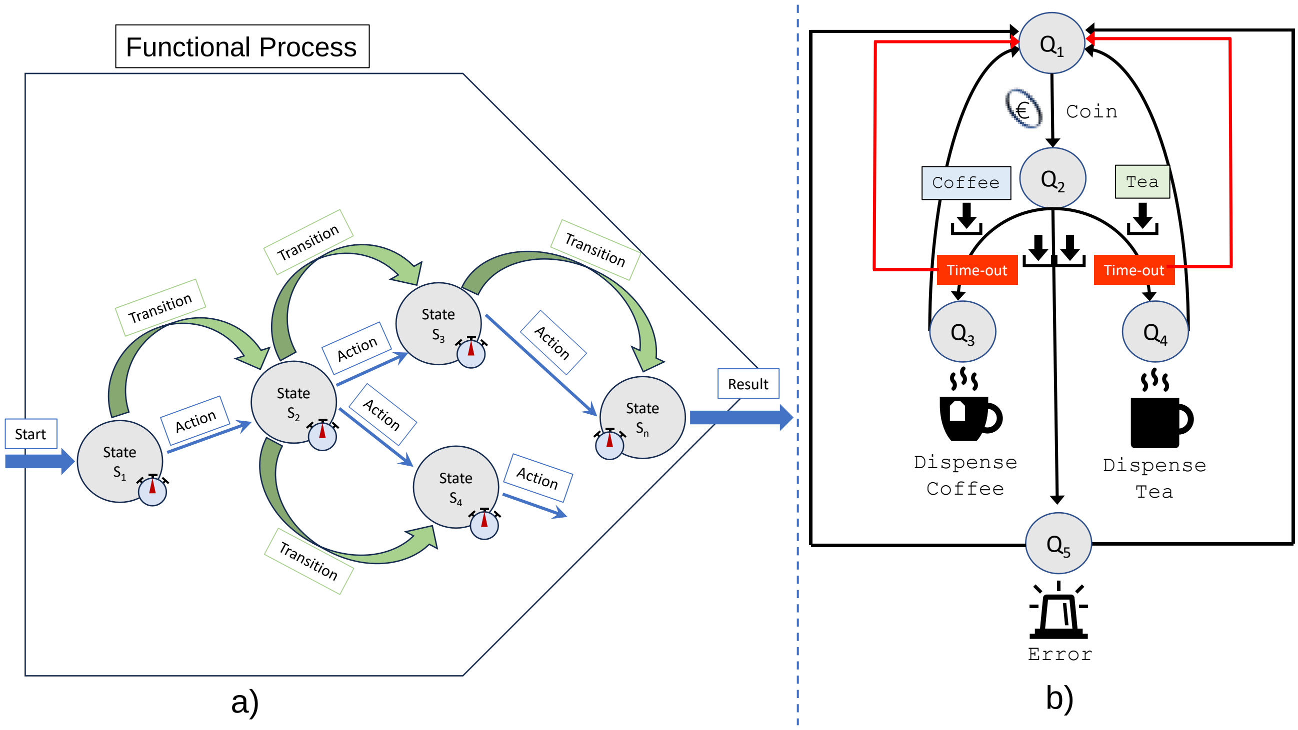


Figure 4: Transition Systems

Figure 4b shows the example of a vending machine that is often used as a (much simplified) transition system. It has five states: Q_1 (= «Waiting for coin»), Q_2 (= «Waiting selection»), Q_3 (= «Coffee»), Q_4 (= «Tea»), Q_5 (= «Error»). The transitions are represented by arrows, including time-out after coin insertion and pressing both buttons simultaneously.

Timed Petri Modules and Inter-Modular Connectors

Context: Several realizations of the Petri Net idea exist. The one best suited for this architecture has been developed by Reggie Davidrajuh (https://www.davidrajuh.net/reggie/). It is applicable to large discrete systems and allows arbitrary system structures.

The functionality and quality properties of the system are implemented using "Timed Petri Modules" (Popova-Zeugmann, 2016; Wang, 1998) and "Inter-Modular Connectors" (Davidrajuh, 2021, Figure 5).

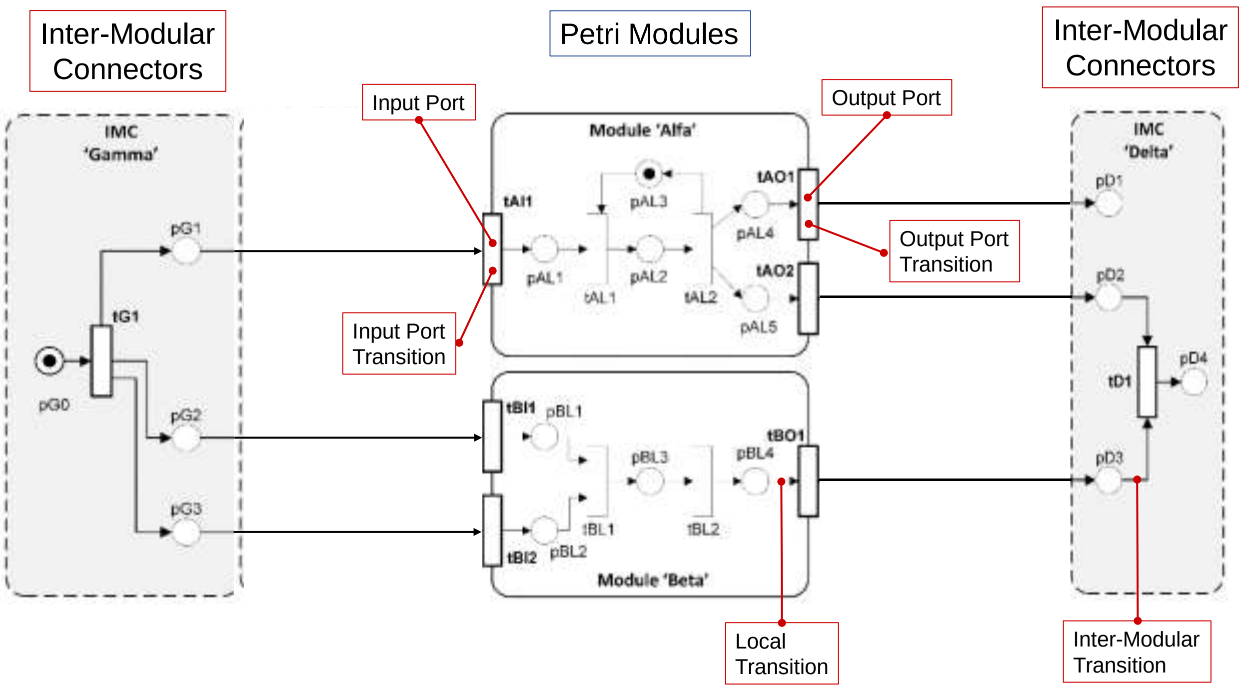


Figure 5: Timed Petri Modules and Inter-Modular Connectors

The Timed Petri Modules feature all the constructs and properties of Petri Modules with time (e.g., Girault, 2010). They implement the functionality and data. The interconnections of the Petri Modules specified by the process algebra are implemented by the Inter-Modular Connectors (IMC). These two building blocks give the architecture designer a high level of flexibility and allow any structure (not only hierarchical) to be defined.

The process algebra does not specify the system architecture. The distribution of functionality to the individual Petri Modules (Partitioning, cohesion, and coherence, etc.), the coupling of the Petri Modules by the Inter-Modular Connectors (Interfaces, loose coupling, etc.) must be designed by a specialized system/software architect. Fortunately, proven, well-documented architecture principles and patterns (Figure 6) are available to construct a dependable, maintainable, and evolvable architecture (e.g., Murer et al., 2014/Furrer, 2019/Furrer, 2022, Transformation Layer A below).

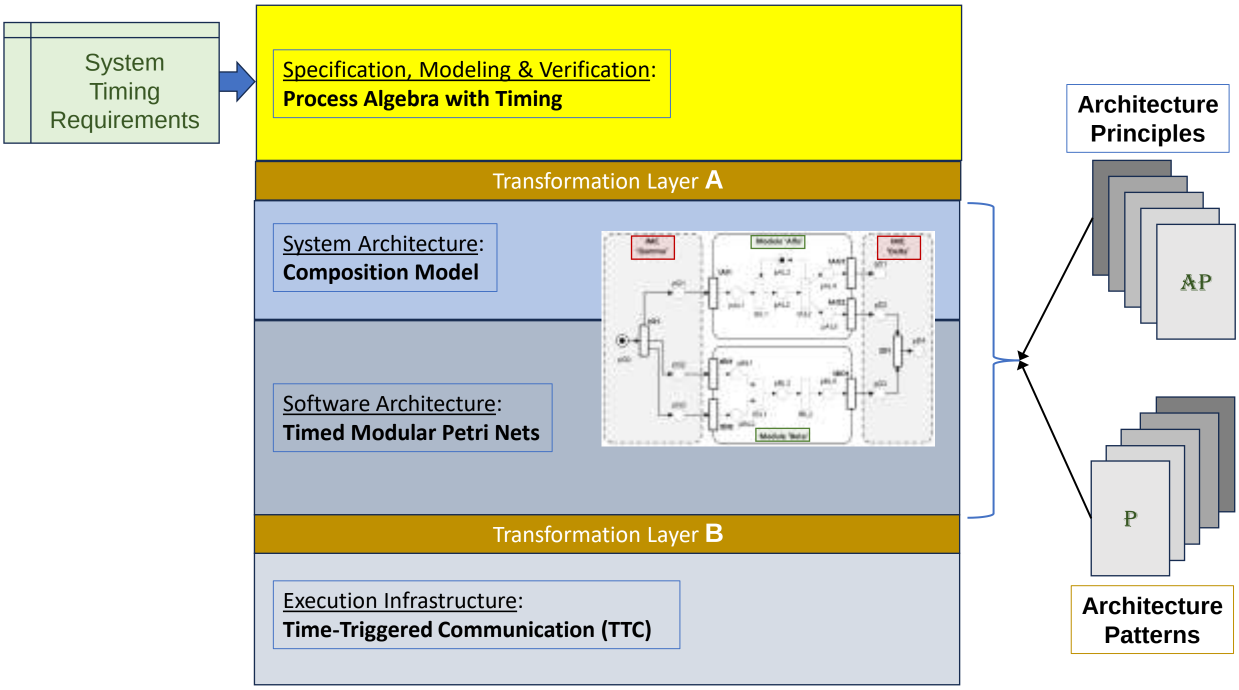


Figure 6: Software Architecture

Transformation Layer A

Context: While the four functional layers in Figure 6 use well-known, well-documented, and proven technologies (Such as transition processes, process algebras, timed Petri Nets, the IMC composition model, and time-triggered communications), the two transformation layers are new concepts. The transformation layer A maps a timed transition system onto a timed Modular Petri Net. Although some literature exists on this specific topic (e.g., Badouel et al., 2015 / Devillers et al., 2022 / Best et al., 2024 / Cortadella et al., 1995 / Goltz, 1990), this transformation layer becomes a research topic – especially concerning timing implementation.

The transformation layer A has two transformation paths (Figure 7):

Transformation Path 1 (Architecture, Figure 7):

The structural organization of the modular Petri Nets is of the highest importance, i.e., strict adherence to proven architectural principles, such as modularization, correct partitioning (respecting cohesion and coherence), loose coupling, and separation of concerns (e.g., Furrer, 2019; Platzer, 2018). This design of the adequate structure is independent of the formal specification of the system and must be carried out by very experienced software architects. Transformation path A requires a strong architecture governance in the IT organization (e.g., Murer, 2014 / Bell, 2023). Once the Petri Modules/IMC structural architecture has been defined, the states and transitions that are to be encapsulated by each Petri Module are selected (Figure 7). Once all states, transitions, and quality properties are transferred from the timed transition system to the timed Petri Module system, the duty of transformation path 1 is completed. Today, transformation Path 1 is state-of-the-art in methodology and architecture knowledge.

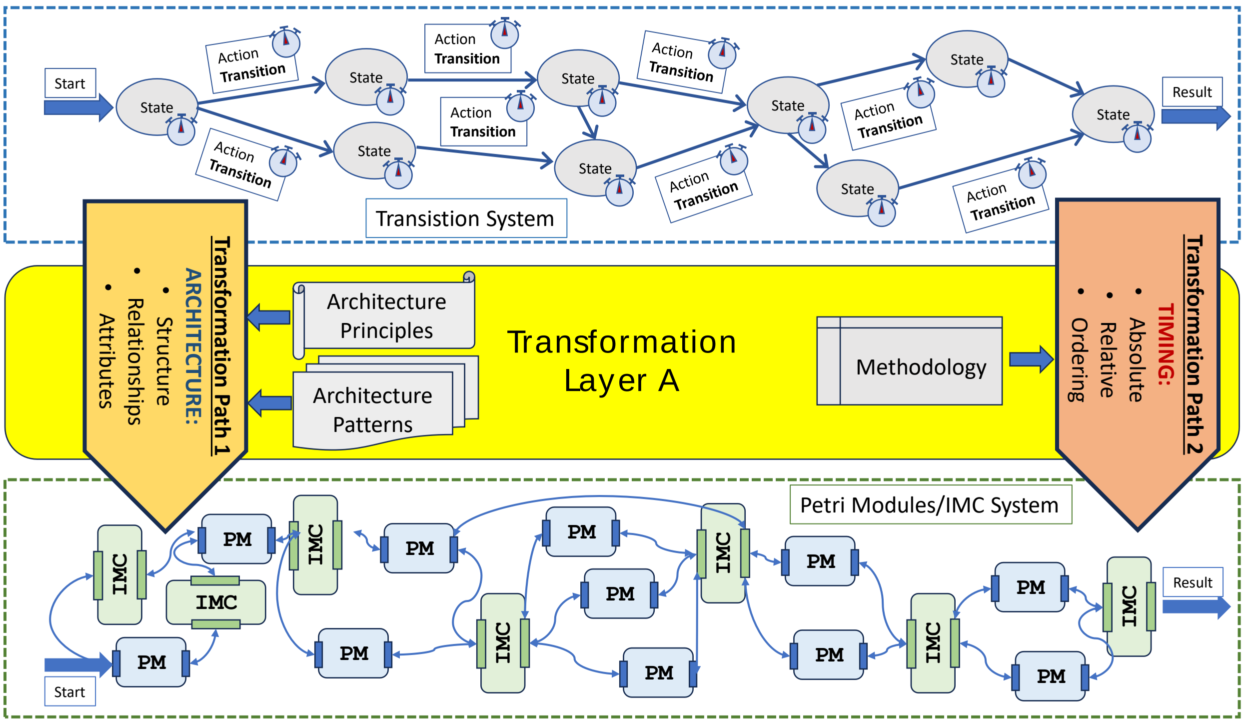


Figure 7: Elements of the Transformation Layer A

Transformation Path 2 (Timing, Figure 7):

Timed transition systems (e.g., Furia et al., 2012, chapters 7.3 & 7.4 / Henzinger et al., 1991 / Hale et al., 1994) and timed Petri Nets have different formal notations for time representation (e.g., Furia et al., 2012, chapter 8 / Wang, 1998 / Penczek et al., 2006). These different notations have differing expressiveness, and suitable notations must be selected for this application.

The transformation path 2 transcribes the transition system timing information to the Petri Net timing information (e.g., Best et al., 1998), including all constraints. Promising initial work has been done on such transformations (e.g., Khomenko et al., 2022 / Huang et al., 2021), but more consolidating research is needed for this transformation path, focussed on the proposed architecture.

Transformation Layer B

Context: The responsibility of the transformation layer B is to select one or more Petri Modules and use them to form a task (Figure 8). This includes correctly transforming not only the functionality and data, but also the timing and the quality properties.

The transformation layer B has two transformation paths (Figure 8):

Transformation path 3 (Architecture):

Transformation path 3 selects one or several coherent Petri Modules, allocates them to specific tasks, and uses the IMCs to define the relationships from task to task and from task to the environment. While the adequate architecture (structure, relationships) has already been defined by transformation path 1, the transfer of functionality/data/relationships/quality attributes from the Petri Module system to the task universe by the transformation path 3 must at least preserve – preferably improve – the quality of the software architecture. This means, again, strict adherence to proven architectural principles and patterns, such as modularization, correct partitioning (respecting cohesion and coherence), loose coupling, and separation of concerns, etc. (e.g., Furrer, 2019 / Richards et al., 2025 / Martin, 2017 / Cervantes, 2024 / Khononov, 2025 / Fettke et al., 2022). Once all Petri Modules/IMC are transferred to the task structure, the duty of transformation path 3 is completed. Today, transformation Path 3 is state-of-the-art in terms of both methodology and architecture knowledge.

Transformation path 4 (Timing):

Transformation path 4 transfers the timing specifications from the Petri Net module system to the task universe, i.e., to the implementation level. Timing in Petri Nets is introduced associated with places, transitions, or both. Some work has been done on software implementations of timed Petri Nets (e.g., Girault et al., 2010 (Chapters 20 & 21 / Ferscha, 1994 / Barad, 2016 / Moreno et al., 2006 / Andrezejwski, 2001). However, neither approach is sufficient for the application to the transformation path 4. Therefore, transformation Path 4 needs more research, specifically directed to the proposed architecture.

… and one feedback path (Timing adjustments): Timing Feedback

The applications prescribe the timing requirements for the system (Processes in Figure 1). At the moment of timing specification, there is no guarantee that their successful implementation will be feasible (e.g., Klemm et al., 2021 / Philippou et al., 2007). The following obstacles may appear:

- Some tasks may have an unexpectedly large WCET (Worst Case Execution Time);
- The task system is not schedulable (TTA);
- The physical communications channel’s transmission times negatively impact timing;
- The system does not provide sufficient resources to handle concurrency and latency;
- Correct error and fault handling require more resources than expected;
- etc.

If the timing can not be implemented in the real CPS, three resorts are possible:

I. Weaken the initial timing requirements (if the applications/processes allow it);
II. Try to modify the architecture (Structure, relationships);
III. Provide more implementation resources.

Once the complete system of timed Petri Net modules has been transferred into tasks and their relationships, and the feasibility of the implementation has been assured, the mission of transformation layer B is complete.

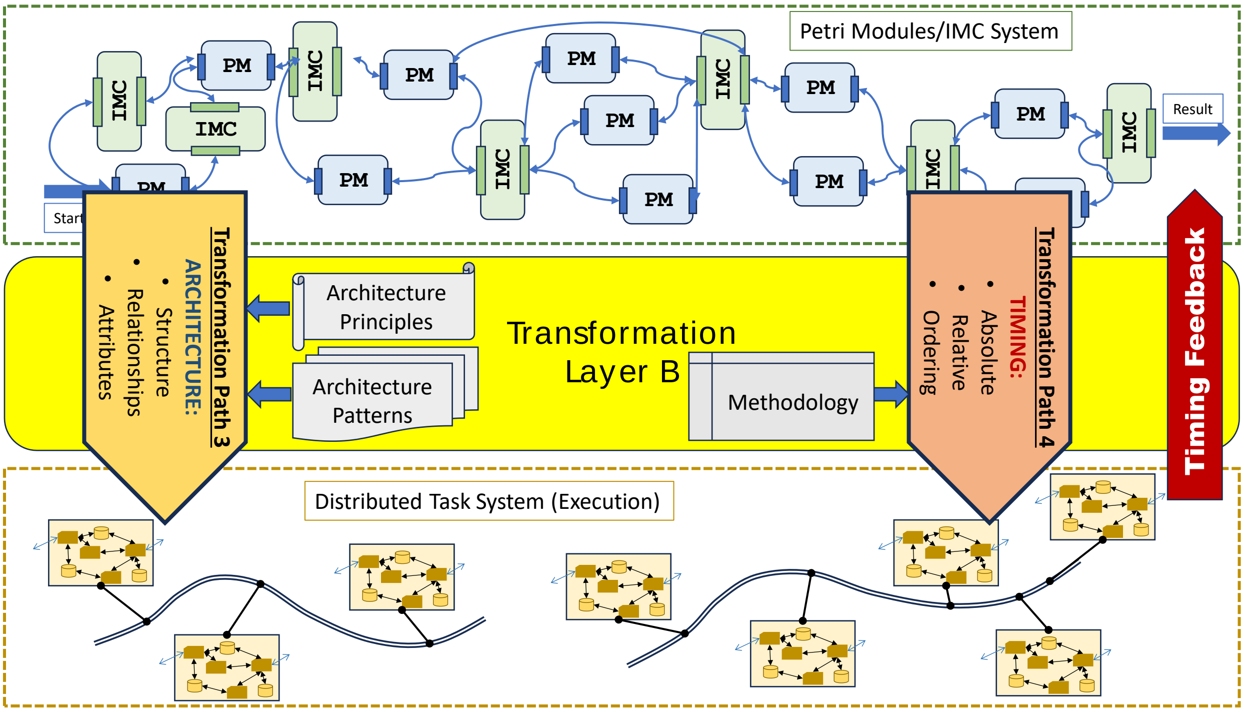


Figure 8: Elements of the Transformation Layer B

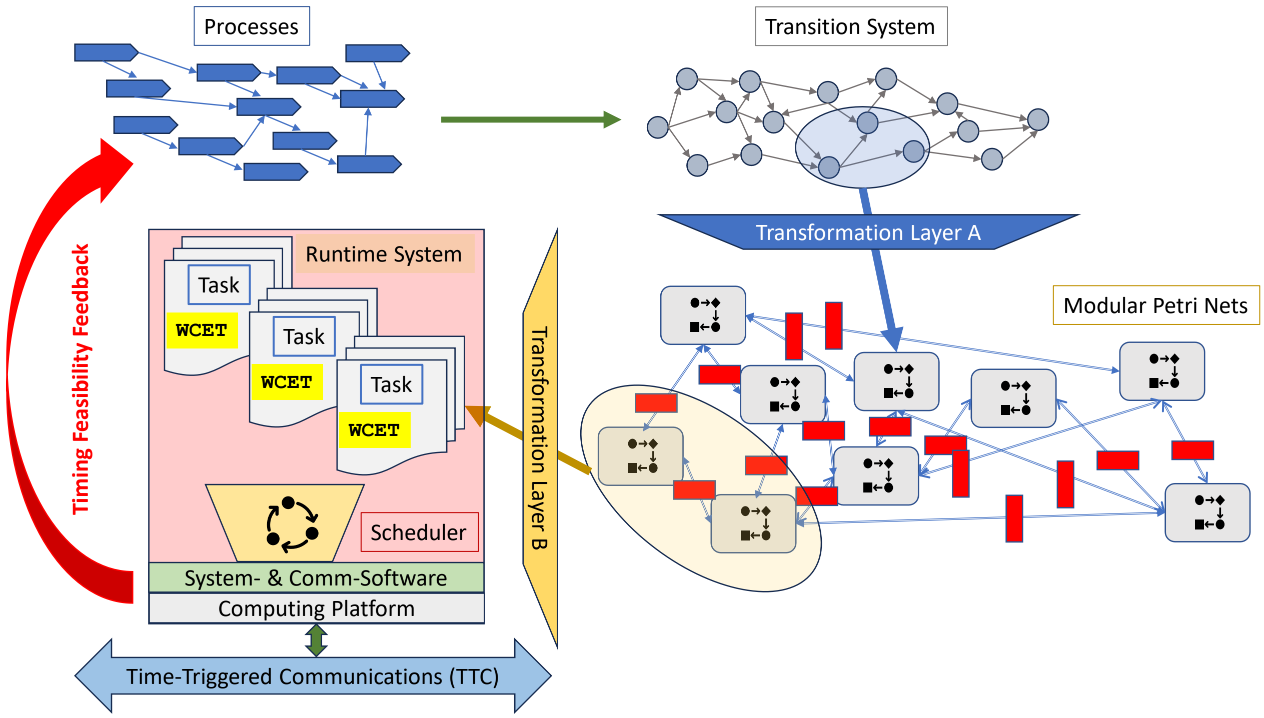


Figure 9: Transformation Layers and Runtime System

Time-Triggered Protocol (TTP) - Time-Triggered Architecture (TTA)

The time-triggered architecture (TTA) defines a fault-tolerant execution platform for large, distributed, embedded real-time systems in mission- and safety-critical cyber-physical applications, such as avionics (e.g., Fuhrmann et al., 2006). It is based on the time-triggered model of computation (Kopetz, 1998 / Kopetz, 2017) and introduces the paradigm of time-triggered communications (TTC, e.g., Kopetz et al., 2003 / Obermaisser, 2012 / Kopetz, 2022/ /Maier et al., 2002/ Rushby, 2005/Buttazzo, 2023). The basic concepts of TTA are shown in Figure 10. Note that the time-triggered communication (TTC) is a paradigm for electronic information exchange (as opposed to the event-triggered communications), the time-triggered protocol (TTP) is the implementation, and the time-triggered architecture (TTA) includes in addition system components, such as scheduler, redundant communication channel, global time synchronization, etc. (Figure 10).

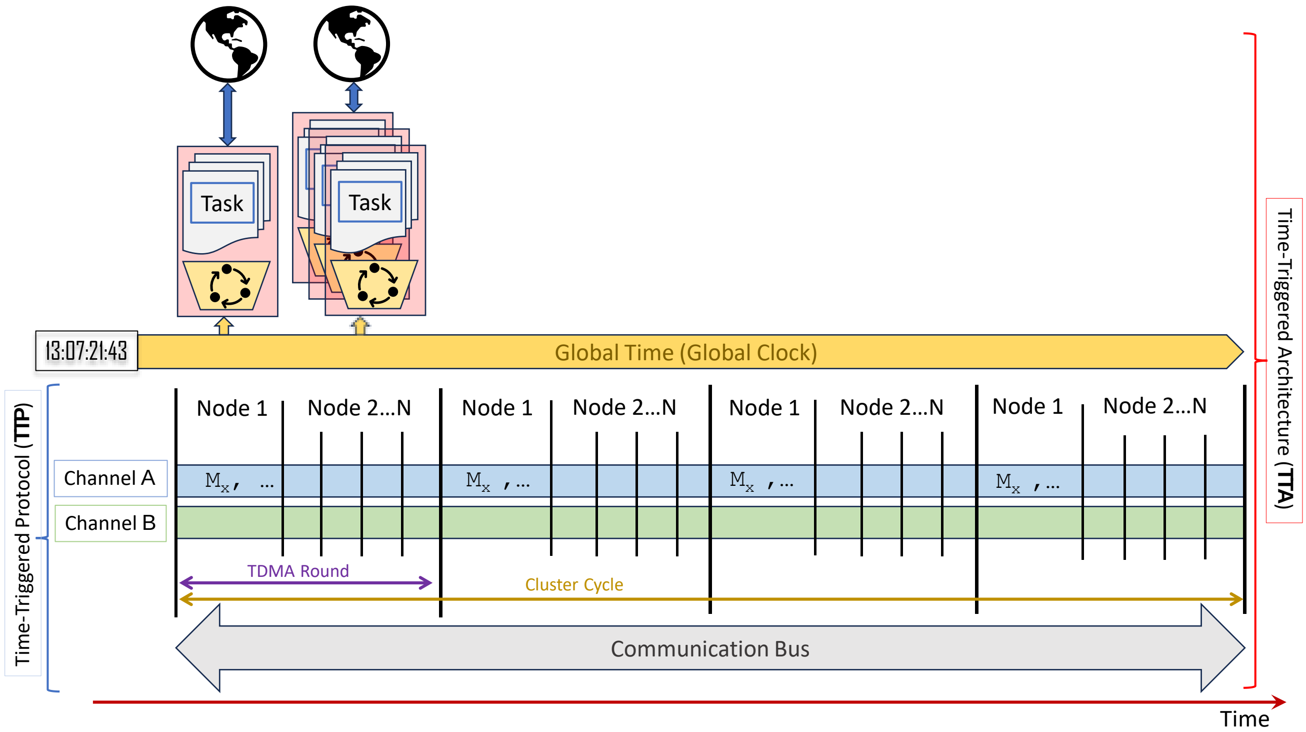


Figure 10: Time-Triggered Architecture

The Figure 10 introduces the following elements (From lowest to highest):

(1) A redundant communication bus that allows the exchange of messages. Initially, a TDMA (Time Division Multiple Access)-scheme was used in the TTP. Later – forced by industry standardization – TTP was implemented on top of more communication schemes, such as CAN (Führer et al., 2000), Ethernet (Kopetz et al., 2005), and FlexRay (Shaw et al., 2008);

(2) Two time-triggered protocols (TTP), managing the exchange of messages between the N nodes in the network, are implemented on top of the two communication channels, providing the necessary redundancy for safe operation. TTP provides fault-tolerant message transport with a fixed schedule at known times and minimal jitter by employing a TDMA (Time-Division Multiple Access) strategy;

(3) A protocol to establish a global, synchronized time in all the nodes. TTA provides system-wide, fault-tolerant, and distributed clock synchronization, establishing a global time base without relying on a central time server.

(4) The runtime systems in each node, i.e., a set of tasks governed by a scheduler.

(5) Several algorithms for system functions (Obermaisser et al., 2012, Chapter 4):

i. Clock synchronization,
ii. Startup and Restart,
iii. Diagnostic Services,
iv. Error Detection and Fault Isolation,
v. Configuration Service,
vi. Schedule Generation and Schedulability Analysis

(6) The interfaces for the interaction of the tasks with the physical world (Sensors, Actuators).

The Time-Triggered Protocol is a deterministic, verifiable, well-analyzed message exchange scheme for fault-tolerant, distributed systems (e.g., Rushby, 2002). Therefore, it forms a predictable foundation for the execution platform in Figure 6.

Worst-Case Execution Time (WCET)

Each program (= a piece of code) has a worst-case execution time (WCET, e.g., Lokuciejewski, 2011). The worst-case execution time (WCET) of a program is the maximum amount of time the program could take to execute on a specific execution platform, i.e., the longest path through the program. Unfortunately, the WCET determination corresponds to the halting problem and is therefore not generally solvable. Estimation methods, such as simulation and code analysis (e.g., Franke, 2016 / Ferdinand et al., 2004), must be used to obtain valuable results. For time-sensitive software, the WCET of each program/module/task must be determined with sufficient accuracy (e.g., Wolf, 2002).

Runtime System and Task Scheduling

The resulting runtime system is shown in Figure 9. It consists of a set of tasks, system- and communications software, a computing platform (today often a cached, multicore CPU), the

TTC bus, and a task scheduler. The scheduler orchestrates the sequence of execution of the tasks in the distributed nodes of the system.

Except for the scheduling, all elements of the conceptual architecture in Figure 6 have been chosen due to the predictability and verifiability of their correct timing behavior. Scheduling, preemption, and resource sharing may cause timing uncertainties and must be analyzed and implemented very carefully. A rich literature related to building, verifying, and operating predictable, hard real-time computing platforms exists (e.g., Buttazzo, 2024 / Gliwa, 2022 / Obermaisser, 2012 [Chapter 15] / Ayman et al., 2009 / Antolak et al., 2023). There is no space to handle this topic, only to raise awareness.

Cyber-physical systems need global time, i.e., a system-wide, precise, and synchronized common physical time scale in all elements of the CPS (Shrivastava et al., 2016 / Broman et al., 2013 / Rajeev et al., 2012). In the conceptual architecture of Figure 2, the Time-Triggered Architecture provides the global clock (Figure 10 / Obermaisser, 2011, Chapter 4).

Mixed-Criticality Systems

Many CPSs are “mixed-criticality systems”, i.e., they contain time-sensitive processes/parts and non-time-sensitive processes/parts. The system design must be based on solid partitioning and loose coupling between the two criticality regions.

Timing Verification

The final truth of timing correctness lies in the runtime system (Lowest layer in Figure 6). Only if the runtime system strictly adheres to all timing specifications in all operating conditions can it be qualified as safe. The strong formalism and model-checking capabilities of the 3 top layers in Figure 6 ensure high confidence in the system timing conformance with the specifications because of the formal verification. Process algebras, transition systems, and Petri Nets allow the verification of their timing properties (e.g., Becker, 2020 / Willemse, 2003 / Camargo, 1998 / Corradini et al., 1999 / Philippou et al., 2007 / Penczek et al., 2006 / Wolf, 2002).

Timing verification on the lowest layer in Figure 6 (Runtime system) requires measurements, tracing, statistics, analysis, and assessment (e.g., Rohr, 2015 / Becker, 2020). Runtime verification, especially for the timing, is a challenging task but sufficiently researched (e.g., Colombo et al., 2022).

Real-Time Calculus (RTC)

A promising development for formalizing the timing behavior and formal verification of the runtime system is the real-time calculus RTC (e.g., Guan, 2018 / Thiele et al., 2000 / Two Examples: Chokshi, 2010 / Bazzal et al., 2020). The key concept in RTC is the Greedy Processing Component (GPC, Figure 11). The GPC accepts input events, launches the appropriate processing, and outputs the processed event stream. The event streams are formalized by arrival curves based on the number of events arriving at an interval (one for the lower bound, the other for the upper bound). The resources consumed to process the input events are also formalized by service curves based on the amount of resources consumed in an interval Δ, one for the lower bound, the other for the upper bound.

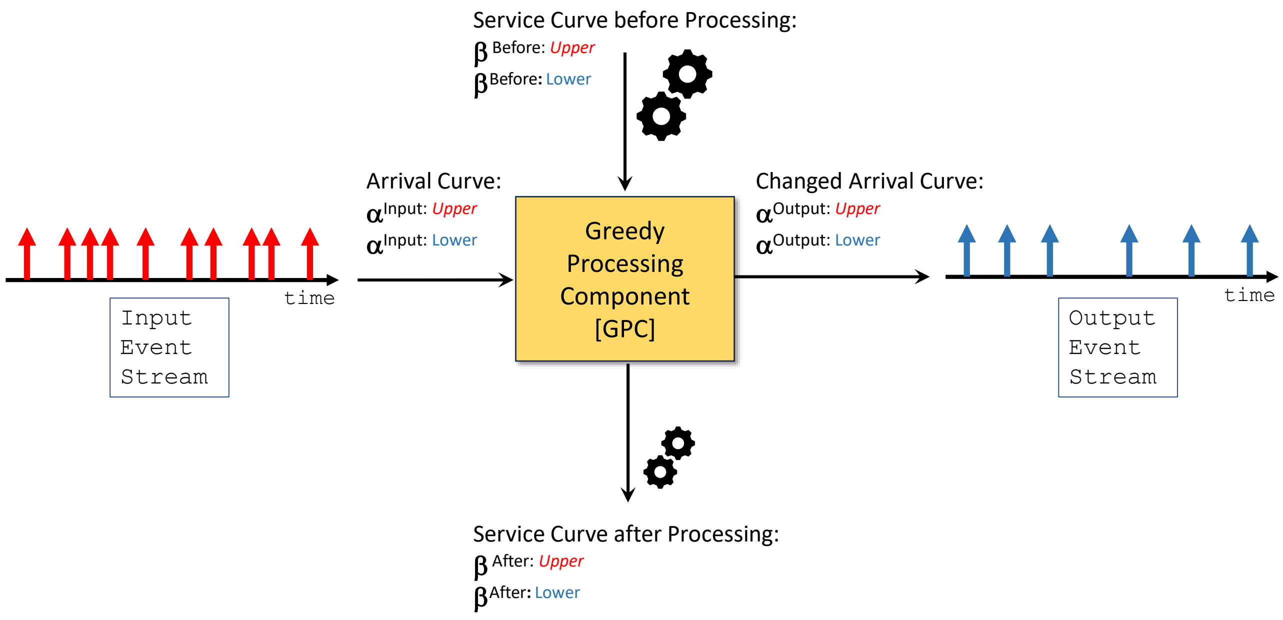


Figure 11: RTC Key Concept – Greedy Processing Component (GPC)

For the arrival and service curves, operators are defined to build compositions of GPCs and thus describe systems of arbitrary complexity. The benefits of the RTC include the formalism for determining bounds for execution, communication, queues, and buffer sizes. Additionally, the schedulability of multitasking software systems can be determined using Real-Time Calculus (RTC).

Runtime Monitoring

As a last defense against timing violations, runtime monitoring can be used. Whereas runtime verification aims to check specific parameters of the program execution, such as the execution times of a set of tasks, runtime monitoring supervises the system in order to detect anomalous or dangerous behavior. If anomalous behavior is detected, the system may automatically take protective actions, thus trying to avoid safety accidents or security incidents. Machine learning algorithms are often used for anomaly detection. (e.g., Furrer, 2023).

Results

Strict adherence to timing requirements is a crucial precondition for the safety of cyber-physical systems. Therefore, the software controlling the CPS becomes time-sensitive. The conceptual system architecture is the foundation for the assurance of timing requirements in a CPS. Only an adequate system architecture allows the formal specification, verification, modeling, and implementation of timing requirements on all levels and for all process steps.

This paper proposes a novel timing-aware architecture composed of well-known technologies: process algebra for modeling transition processes, Petri Nets for implementation, and time-triggered communications as the execution platform. The timing-aware 4-layer architecture is presented as a conceptual 4-layer model. From this model, many research topics follow.

Open Questions and Future Work

- Develop a complete and consistent metamodel to ensure the conceptual integrity of all layers in Figure 2 (e.g., Gonzalez-Perez et al., 2008)
- Choose and agree on a semantic and notation for a suitably timed process algebra. Codify it as an industry standard;
- Choose and agree on a semantic and notation for timed transition systems. Propose it as an industry standard;

- Choose and agree on a semantic and notation for a timed Petri Nets (Preferably based on Davidrajuh, 2021). Propose it as an industry standard;
- Develop, discuss, and document a modeling methodology for systems based on Figure 6 (Metamodel, notation, semantics, graphical representation, etc.);
- Define a methodology, principles, and metrics for the transformation layer A;
- Define a methodology, principles, and metrics for the transformation layer B;
- Integrate the formalism of real-time calculus (RTC) into the architecture of Figure 6;
- Investigate the applicability of the (possibly extended) conceptual architecture of Figure 2 to continuous and hybrid cyber-physical systems (e.g., David et al., 2010 / Gu et al., 2005 / Bera et al., 2014 / David et al., 2010);
- Demonstrate the capability of the conceptual architecture (Figure 2) for closed-loop CPS (e.g., Pasandideh et al., 2023 / Núñez-Alvarez et al., 2023);
- Does the conceptual architecture (Figure 2) have the capability to generate the most efficient solution regarding resources? (Rodriguez, 2013 / Jarabo, 2024 / Shi, 2023);
- Is adding more resources until timing constraints can be satisfied always feasible?

Conclusions

For mission-critical cyber-physical systems, the correct specification, implementation, and execution of complete timing specifications is a *correctness property* rather than a *quality attribute*. To answer this challenge, the underlying system architecture must provide formal, verifiable, and complete timing constructs on all levels. This paper proposes a novel, four-layer architecture with sufficient formalism based on established technologies to handle and verify timing in a Cyber-Physical System (CPS).

Declarations

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Data availability does not apply to this article as no new data were created or analyzed in this study.
Ethical approval and consent are not relevant to this article type.

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