capacitively coupled with the input voltage $V_{\rm i}$ through an 8-nm-thick ${\rm Al}_{x}O_{y}$ layer. Small tunnel junctions connect the transistors to power lead, output, and ground. A load capacitor connects the output to the ground to suppress charging effects. Two tuning gates, with voltages $V_{\rm g1}$ and $V_{\rm g2}$, are used to tune the induced charges on the two islands.

The device was fabricated on a thermally oxidized silicon substrate using a high-resolution electron-beam pattern generator at 100 kV. A bottom layer of Al served as the lower electrodes of the gate capacitors and the load capacitor. An $\text{Al}_x O_y$ dielectric layer was created upon these electrodes by oxidizing the sample in an O_2 plasma. A second (upper) layer of Al forms the aluminum islands and the leads; on this layer the four tunnel junctions were defined by shadow evaporation.

The inverter operates such that one SET is conducting while the other is in Coulomb blockade, depending upon the input voltage. Shifting the input voltage alters the induced charge on the SETs by a fraction of an electron and inverts the input.

Measurements were performed in a dilution refrigerator with a base temperature of 25 mK, while suppressing superconductivity using a 1 T magnetic field. The input–output behavior of this device varied greatly depending on the two gate voltages $V_{\rm g1}$ and $V_{\rm g2}$. A maximum voltage gain of 2.6 was achieved at 25 mK, which remained larger than one up to about 140 mK, confirming that the device operated as designed. This is the highest temperature for which voltage gain in a SET has been achieved.

Inverters are building blocks for other digital logic elements, including NAND or NOR gates, SRAMS, and ring oscillators which should be producible from variations of or combinations of SET inverters. To date, however, there is no automatic method that would allow optimization of performance by adjusting gate voltages on-chip. The researchers state that "this is probably the largest problem inhibiting the further development of this sort of logic."

Wirawan Purwanto

Electrophoretic Approach Results in 3D Assemblies of Gold Nanoparticles

A promising synthetic path for the preparation of three-dimensional (3D) films of gold nanoparticles has been described by a team of researchers at the Notre Dame Radiation Laboratory. In the February issue of *Nano Letters*, they report that highly porous nanostructured

films were assembled using an electrophoretic approach. The film thickness could be controlled by varying the concentration of gold colloids in solution and the applied voltage. The particles did not aggregate, as evidenced by the strong surface plasmon band.

The electrophoretic deposition method subjects colloidal solutions of tetraoctylammonium-bromide-capped gold nanoparticles of 5-10-nm diameter in toluene to a dc electric field (50-400 V). This results in a negative charge on the gold nanoparticles, which are then driven toward the positively charged electrode surface. In this study, the composite electrode consisted of an optically transparent electrode (conducting glass) onto which was cast a nanostructured TiO₂ film. The porous TiO₂ film is required for good deposition of the gold nanoparticles. The nanoparticles form a 3D array on the electrode surface without undergoing aggregation or inducing bulk film effects.

"We believe that the capping material acts as a spacer between the adjacent particles in the film," said senior research scientist Prashant V. Kamat, who conducted this study together with Nirmala Chandrasekharan, a postdoctoral re-

searcher at the Radiation Laboratory. "The films exhibit a strong surface plasmon band, which indicates that they retain their identity as individual nanoparticles." The thickness of the films can be controlled by adjusting the concentration of the colloidal solutions and the applied voltage.

The nanostructured films obtained by electrophoretic deposition are stable in atmosphere and highly porous, thus providing a large surface area for anchoring electroactive or photoactive molecules.

"To the best of our knowledge, this is the first report that highlights the feasibility of achieving relatively thick nanoporous gold films with minimal aggregation effects," said Kamat. "The ability to assemble gold nanoparticles as a 3D array of clusters opens new avenues for designing sensors and optoelectronic nanodevices. Nanostructured gold films of high surface area also have potential applications in catalysis and photoelectrochemistry."

Cora Lind

Self-Interstitial Clusters Diffuse Extremely Fast in Crystalline Silicon

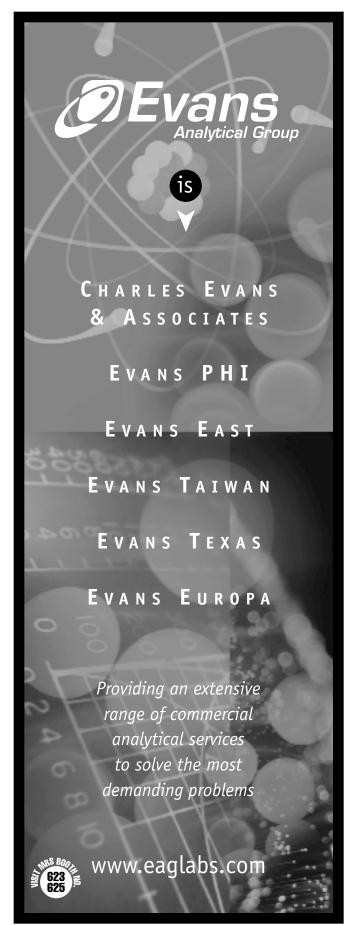
Theoretical studies of the self-interstitial defect I in crystalline silicon show that





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several small I_n clusters exhibit unexpected dynamic behavior and could dominate the precipitation of I's under conditions of supersaturation. In the February 12 issue of *Physical Review Letters*, S.K. Estreicher and M. Gharaibeh of Texas Tech University, P.A. Fedders of Washington University, and Pablo Ordejón of Institut de Ciència de Materials de Barcelona report that *ab initio* molecular-dynamics (MD) simulations show that the di-interstitial (I_2) clusters and one particular tri-interstitial (I_3) cluster diffuse remarkably fast, too fast to be seen experimentally.

Ab initio MD simulations with pseudo-atomic basis sets (SIES-TA) were performed in periodic supercells containing 64 (with four k-points), 128 (one k-point), and 216 (one k-point) host atoms. The basis sets varied from minimal (one set of s and p orbitals per Si atom) to double-zeta-plus polarization (two sets of s and p orbitals plus one set of d orbitals per Si atom). The electronic energy was obtained using density-functional theory within the local density approximation. The exchange-correlation potential was that of Ceperley-Adler as parameterized by S. Perdew and A. Zunger. Norm-conserving pseudopotentials in the Kleinman-Bylander form were used to remove the core electrons from the calculations. A time step of 2.0 fs was used in all the simulations.

After simulated quenching starting from many possible initial configurations, the researchers determined that only one configuration of I_2 and two configurations of I_3 are stable. Several structures for I_4 were also obtained. Constant-temperature MD simulations at 1000 K and 77 K show that I and I_4 behaved as expected, vibrating around their equilibrium sites. In the metastable I_3^b cluster, the three self-interstitials continuously exchange positions without motion of the center of mass of the defect. However, I_2 and I_3^a diffuse with remarkable ease. Both clusters are centered around a single bond-centered site and two (for I_2) or three (for I_3) I's join forces to displace the same host atom, thus facilitating the exchange process and allowing fast diffusion.

DONALD F. CARTER

Aluminum Induces Crystallization in Amorphous Silicon at 150°C

Aluminum-induced crystallization (AIC) has been observed in amorphous silicon ($\alpha\textsc{-Si:H}$) films. As reported in the February issue of $\it Electrochemical$ and $\it Solid-State$ Letters, researchers at the University of Arkansas deposited Al onto $\alpha\textsc{-Si:H}$ films and annealed them. Transmission electron microscopy (TEM) and x-ray diffraction (XRD) showed that crystallization occurred at 150°C and above. No further crystallization occurred after the Al was removed.

The α-Si:H films were deposited by ultrahigh-vacuum plasma-enhanced chemical vapor deposition (PECVD) onto carbon-coated nickel grids. A 50-nm-thick Al film was then deposited by vacuum evaporation. Next, the films were annealed at temperatures between 100°C and 250°C under 2 mTorr vacuum. The Al was removed by KOH etching.

TEM of a film annealed at 140°C for 20 min showed no large nucleation sites. The electron diffraction pattern (EDP) shows broad Si halos indicative of amorphous material. TEM of a film annealed at 150°C for 30 min, however, shows the film has completely crystallized into randomly oriented polycrystalline silicon, with grain sizes ranging from 0.2 to 0.5 µm. The EDP clearly shows the 〈111〉, 〈220〉, and 〈311〉 rings. At lower magnification, the micrograph shows a honeycombnetwork morphology, which may indicate that the growth pattern of the polycrystalline silicon was dendritic. Similar features have previously been observed by other researchers.

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