International Journal of Microwave and Wireless Technologies

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GaN/SiC V-band 10 W high-power amplifier for inter-satellite communications

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Research Paper

Cite this article: Sivverini G, Meazza A, Traversa A, Colzani A, Fonte A, Moscato S, Oldoni M, Friesicke C (2025) GaN/SiC V-band 10 W high-power amplifier for inter-satellite communications. *International Journal of Microwave and Wireless Technologies* **17**(2), 177–189. https://doi.org/10.1017/S1759078724000655

Received: 31 January 2024
Revised: 10 June 2024
Accepted: 11 June 2024

Keywords:
Active circuits; Power amplifiers; RF front-ends

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Abstract

This manuscript presents a millimeter-wave GaN high-power amplifier (HPA) intended for next generation inter-satellite links (ISLs). The proposed architecture achieves a fractional bandwidth wider than 18% in the V-band spectrum, to deliver a 10 Gbit/s throughput compatible with multi-thousand-km ISLs. Core of the HPA is the monolithic microwave integrated circuits (MMIC) power amplifier which covers the whole 59–71 GHz band with high efficiency through innovative topologies and a cutting-edge gallium nitride on silicon carbide (GaN-on-SiC) process. The MMIC is then parallelized by means of a 1-to-8 splitter/combiner to obtain a V-band 10 W GaN HPA. Measurement results show a peak small-signal gain of 25.6 dB, 6.5% peak power-added efficiency, and a maximum P_{1dB} of 40.3 dBm.

Introduction

Future non-geostationary-satellite-orbit constellations, geosynchronous orbit (GSO) relay satellites and multiple access telecom reconfigurable satellite systems strive for larger and larger data rate to accommodate futuristic applications. Among them, a meshed satellite network architecture allows relay interconnections with reduced number of Earth stations while still providing global coverage. Currently, channel data throughput represents the bottleneck of such systems, hence jeopardizing such architectures. Typical microwave inter-satellite links (ISLs) achieve nowadays 1–2 Gbit/s of data rate through channels only a few tens of MHz wide. Higher capacities can be obtained by means of optical inter-satellite links such as in the European Data Relay Satellite System, in which data relay satellites are maintained in geostationary orbit to relay information to and from non-geostationary satellites, other vehicles and fixed Earth stations that otherwise are not able to permanently transmit/receive data. The use of optical ISLs allows up to 1.8 Gbit/s over long distances and 5.625 Gbit/s over short distances. Optical systems are however hampered by several complex challenges, such as stringent thermal control and pointing accuracy requirements, together with the performance of the components and the high recurring cost of equipment.

An alternative or complementary solution to satisfy the main technical and equipment cost objectives of this technological scenario is the possibility of using radio frequency (RF) data links working with channels significantly larger than before. This is possible in the millimeter-wave frequency region, today available and less-crowded, although careful planning must be undertaken at constellation and inter-constellation level ([1] and its evolutions). The present work addresses the frequency range between 59 and 71 GHz (V-band), which corresponds to an available fractional bandwidth of more than 18%. Such a bandwidth enables >10 Gbit/s data rates for distances of about 5000 km and even higher data rates for shorter distances by using currently available receivers. Aiming at enabling RF ISL at >10 Gbit/s, the main technical objectives are hence: (i) support a very large bandwidth to allow for either a single wideband channel or for multiple parallel simultaneous data channels, and (ii) generate and handle the required high transmit power. This opens the use of higher-order modulations, increasing the number of bits per symbol and ultimately carrying more information per time unit.

An earlier version of this paper was presented at the European Microwave Integrated Circuits Conference and was published in paper [2].

The overall result derived from the combination of the two approaches described before has driven the work presented here: the development of a high-power amplifier (HPA) module capable of 10 W of RF output power with a high power-added efficiency (PAE). The activity involved several technical advancements, outlined in this manuscript: (i) the system-level analysis to select the module architecture, described in the "System overview and V-band HPA

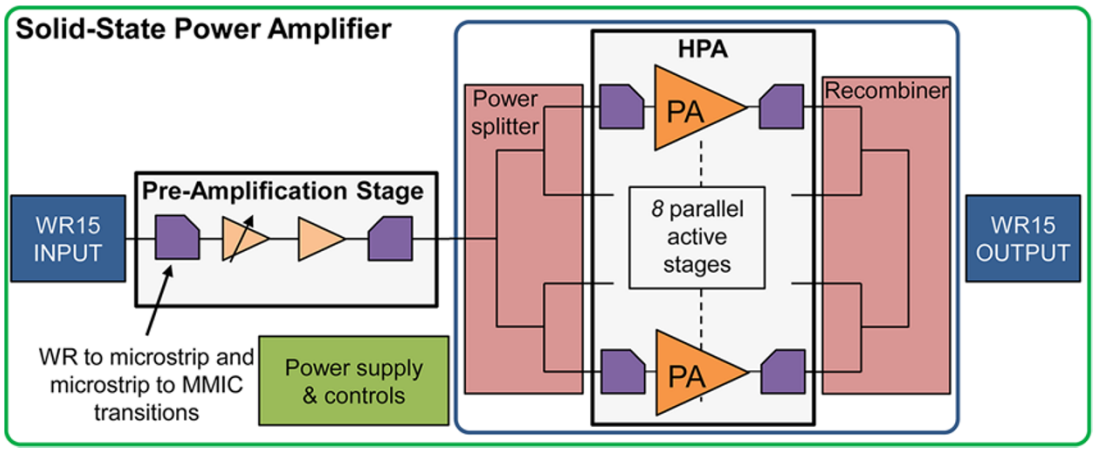

Figure 1. System architecture of the foreseen module.

Table 1. High-level requirements of SSPA with P_{1dB} = 40 dBm and gain = 60 dB

		HPA		
	Pre-amp. stage	Power splitter	Each PA	Power recombiner
Gain (dB)	37.5	−1.5	25.5	−1.5
P_{1dB} (dBm)	29.3	//	33	//

building blocks design" section, as a configuration with multiple paralleled power amplifiers (PAs) [3–7], (ii) the design of all the critical building blocks including the monolithic microwave integrated circuit (MMIC) PA in a gallium nitride technology, input and output (I/O) interfaces, transitions, division-recombination network and mechanical arrangement (described in the "GaN V-band MMIC: Design and measurements" section and the "Splitter/Combiner development" section), and (iii) experimental validation, whose measurement results are described in the "Experimental result" section. Finally, the "Conclusion" section summarizes the achieved results.

System overview and V-Band HPA building blocks design

The proposed V-band HPA constitutes the final stage of a transmitter line up, called solid-state power amplifier (SSPA), able to deliver a 10 W average modulated output power, an overall P_{1dB} of 40 and 60 dB of gain. The SSPA is stable over temperature and aging. A system-level study has been carried out to define the transmission chain and the requirements of each block. From a system perspective, the RF chain is composed of two stages, namely the pre-amplification stage and the HPA. The proposed system architecture of the whole module has been sketched in Fig. 1. An external RF power control loop can be introduced for a fine gain and power adjustment, relying on power detectors after each active stage of the HPA to monitor and control the performance of each stage.

The whole SSPA is enclosed as a module with WR15 I/O waveguide ports. The MMIC design will be presented in the "GaN V-band MMIC: Design and measurements" section and the power splitter and recombiner networks will be described in the "Splitter/Combiner development" section.

According to this study, the following Table 1 summarizes the high-level requirements.

Since the pre-amplification stage is not critical in terms of gain and power handling, the focus of the activities has been the development of the GaN PAs, and the HPA module based on the parallelization of eight amplification stages through a 1-to-8 splitter, as shown in Fig. 1.

GaN V-band MMIC: Design and measurements

In this section, the choice of the technology is briefly discussed, the load pull analysis on the transistors for the PA stages is analyzed, the block diagram and the layout of the MMICs is discussed and the measurement and the simulation results are reported.

Technology overview

The design of a PA with a P_{1dB} close to 33 dBm at V-band and with a high PAE is still a challenge also by using cutting-edge technologies, either gallium arsenide (GaAs) or gallium nitride (GaN) based. The first one is a consolidated process and well covers this frequency range but, as an example on a 100-nm GaAs process, load-pull simulations on Pseudomorphic High Electron Mobility Transistor (pHEMT) devices have shown that, at the upper-edge frequency (71 GHz), 21 dBm of P_{1dB} can be achieved with an associated gain close to 6 dB. Consequently, a 33 dBm P_{1dB} can be achieved by parallelizing 16 Field-effect transistor (FET)s or more, which implies a very difficult design.

Gallium nitride on silicon carbide (GaN/SiC) technology, on the other hand, can reach more easily 33 dBm at P_{SAT}. Unfortunately, the gain of GaN devices vs output power shows early compression compared with GaAs ones. Therefore, P_{1dB} is typically 6–8 dB far from P_{SAT}. This limitation can be sidestepped by exploiting a Doherty topology.

The 100-nm GaN/SiC process from Fraunhofer (IAF), optimized toward high efficiency at millimeter-wave frequencies, has been selected for the V-band PA of this project. Grown on 4-inch semi-insulating 4H-SiC substrates by using metal-organic chemical vapor deposition, the IAF GaN process features high-performance active devices with a current-gain cut-off frequency (f_T) around 110 GHz and a maximum oscillation frequency up to

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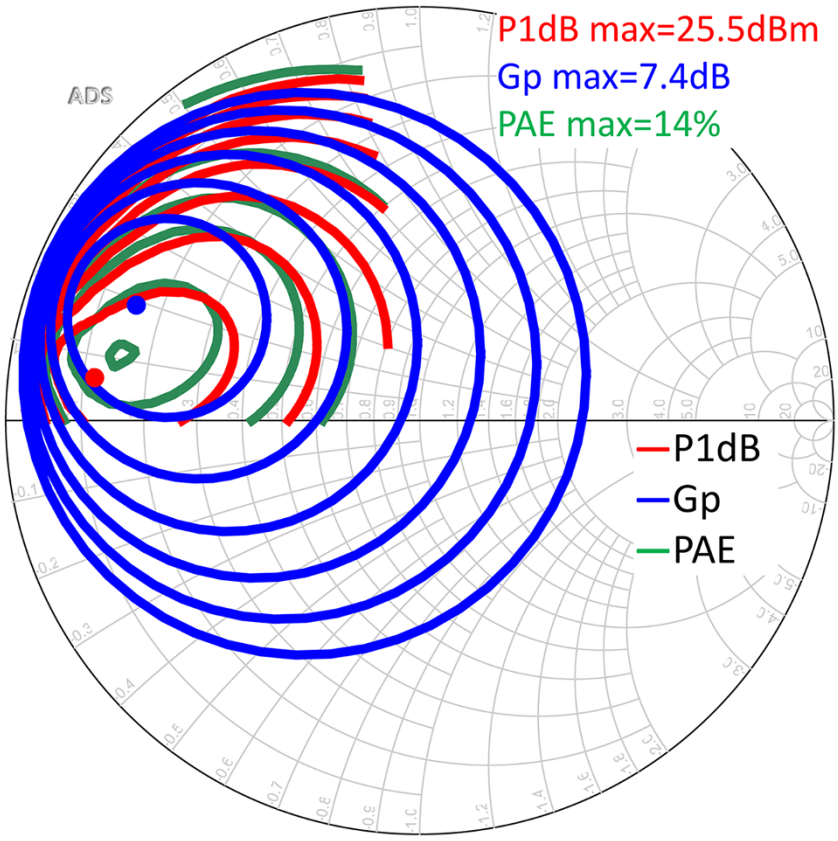

Figure 2. Simulation results of 6 × 90 μm FET at 71 GHz: P_{1dB} (max = 25.5 dBm, step 1 dB), G_P (max = 7.4 dB, step 1 dB) and PAE (max = 14%, step 2%) contours.

290 GHz. The peak output power density is higher than 2 W/mm, according to load pull measurements taken at 38 GHz with a drain supply voltage of 15 V [8].

GaN MMIC design

IAF 100-nm GaN/SiC PDK provides coplanar FET models, with two sources directly connected to the ground plane. This configuration allows to increase the power gain (GP) by minimizing the parasitic inductance effect between sources and ground plane otherwise introduced by backside via-holes. The transistor model is based on the so-called "integral transform" model approach which has been published in papers [9] and [10], and it takes into account trapping. Internally the model has a structure similar to a low-pass/high-pass frequency diplexer, in which the DC/low-frequency response and the trap-affected high-frequency response can both be combined/added to the resulting drain current. The model has a thermal subcircuit (i.e. "electrothermal"). The "baseplate" temperature is provided as a parameter by the user, and the thermal resistance is geometry-dependent (number of fingers, total gate width). For the model extraction, both DC/CW measurements and pulsed measurements are used. The pulsed measurements are taken from two quiescent points, hot-pinchoff and class-AB quiescent point. The "class-AB" quiescent pulse point is a quite high current (on the order of 300 mA/mm) and it is close to the bias that has been used for the V-band PA.

The 6 × 90 μm FET selected for the PA design exhibits the best trade-off among P_{1dB}, GP, and PAE. Moreover, load pull simulation results have shown that the maximum of these three parameters is placed in the same area of the Smith chart, as reported in Fig. 2, allowing an easier design of the output matching networks. Another important point to be taken into account has been related to the derated voltage required by European Space Agency (ESA) and compliant with the ECSS standard [11, 12] for space applications. For this reason, the nominal voltage ($V_D = 15$ V) has been derated by 25%, leading to 11.25 V. Biasing the 6 × 90 μm FET with 11.25 V @ 300 mA/mm the maximum values of P_{1dB}, PAE, and G_P are 25.5 dBm, 14%, and 7.4 dB, respectively. Thermal FEM simulation estimates a junction temperature (Tj) of 153°C with $T_{BASE} = 85$°C. The MMIC complies with the junction temperature limit of $Tj < 160$°C, compliant with the ECSS standard [11, 12] for GaN technologies.

A budget analysis, based on these simulations, has shown that taking into account the losses due to the output matching network, the bondings from die to alumina test-board and the compression of previous stages, four FETs must be parallelized in the last stage in order to achieve a saturated power of 34 dBm. Based on this, the next subsections describe the technique devised to increase the P_{1dB} up to the required value of 33 dBm for the PA.

Several topologies of PAs have been analyzed during the pre-study phase as the continuous class F [13] and other solutions described in [8, 14, 15], that provide very high-level of PAE at P_{SAT}. For this design, a Doherty-like topology has been selected due to the well-recognized and consolidated solution, favorable to a successful first-run design. This topology allows to cover both the wide operating bandwidth (i.e. 59–71 GHz), and the PA specifications given in Table 1: 33 dBm of P_{1dB}, and 25.5 dB of GP. The block diagram of the PA with the details of the FETs size and the current density of each stage is reported in Fig. 3 and Table 2.

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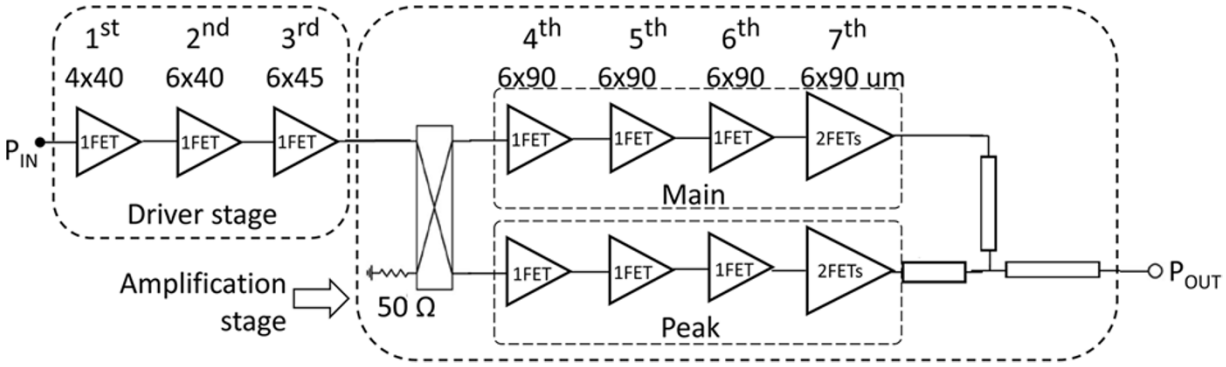

Figure 3. V-band GaN Power Amplifier block diagram.

Table 2. FET sizes and current density at each stage

Stage 1		Stage 2		Stage 3		Stage 4		Stage 5		Stage 6		Stage 7	
n° FET	Size	n° FET	Size	n° FET	Size	n° FET	Size	n° FET	Size	n° FET	Size	n° FET	Size
1	4 × 40	1	6 × 40	1	6 × 45	2	6 × 90	2	6 × 90	2	6 × 90	4	6 × 90
@300 mA/mm		@300 mA/mm		@300 mA/mm		@300 mA/mm		Main:	Deep class AB	@300 mA/mm		@300 mA/mm	
								Peak:	Almost class B				

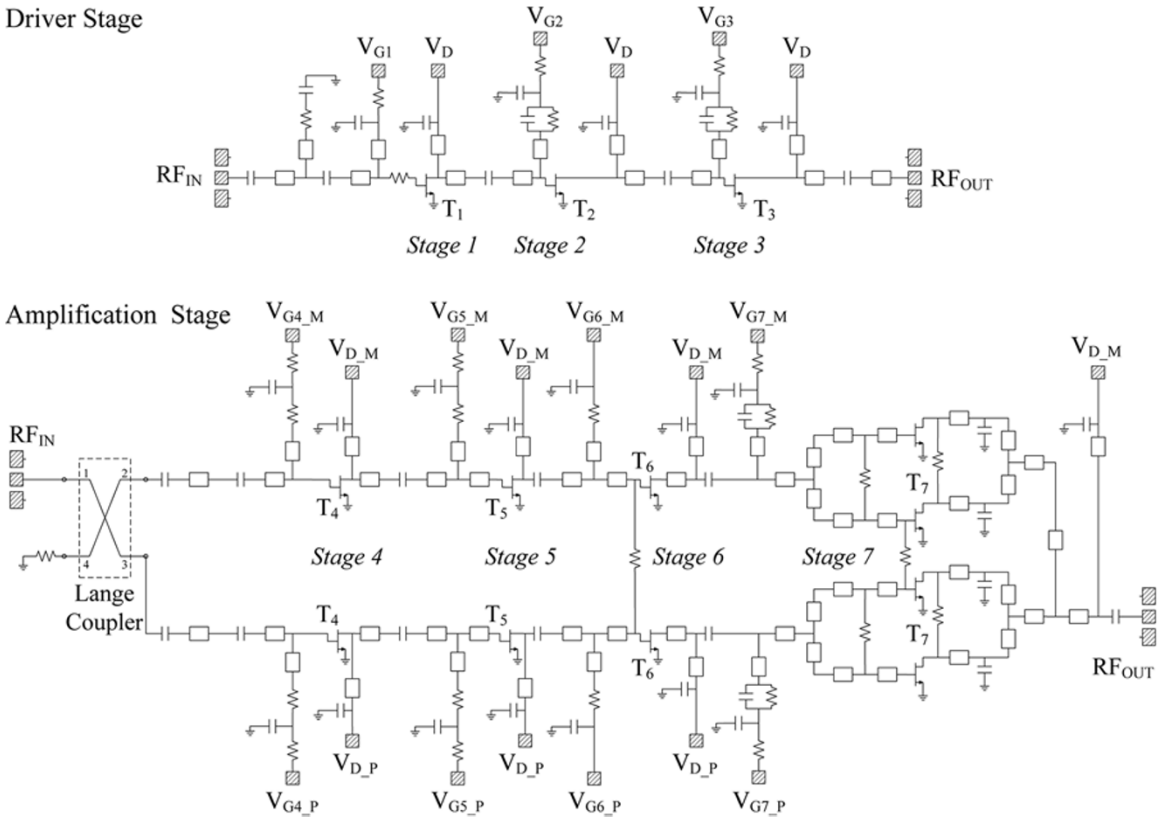

Figure 4. V-band GaN PA: Simplified schematic of driver and amplification stages; the subscripts M and P indicate the main and the P the peak, respectively.

The simplified schematics are reported in Fig. 4. The PA consists of seven stages divided in two sub-blocks. The first three stages constitute the first sub-group, namely the driver stage, that provides a 21 dBm P_{1dB}. The last four stages instead constitute the second sub-group, namely the Doherty-like amplifier. In this sub-group the FETs at stages 4th, 6th, and 7th are biased close to class A (11.25 V @ 300 mA/mm) and the two FETs of the fifth stage are biased in Doherty mode. More in detail, in the fifth stage, the FET in the main branch is biased in deep class AB and the FET in the peak branch is biased almost in class B. It is worth to note that, the design is not a pure Doherty structure due to the strong project requirements in term of P1dB and PAE@P1dB. The PAE@P1dB has been maximized by developing two Expander, the first on the main branch and the second on the peak branch. For these reasons, the

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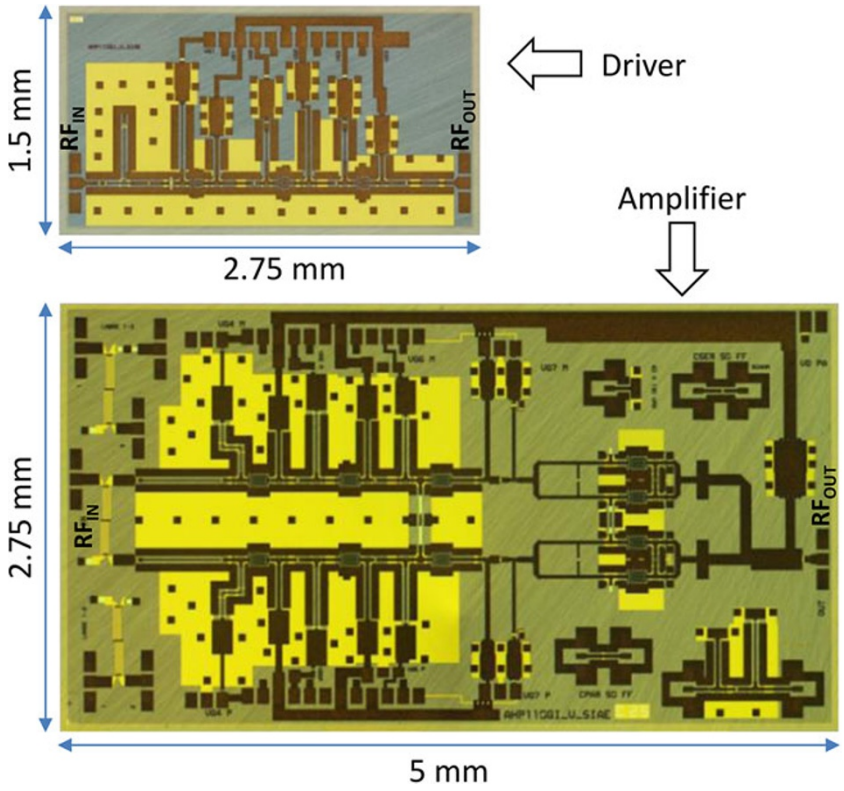

Figure 5. V-band GaN PA: Driver and Doherty amplifier die micrographs.

typical Doherty behavior is not clearly visible due P1dB is close to P_{SAT}, and the double peaks of PAE that usually are 6 dB separated cannot be seen.

To improve the P_{1dB} of the whole chain, the Doherty operating point has been applied only at the fifth stage, as shown in Table 2. This bias configuration allows to achieve the gain expansion necessary to move the P_{1dB} point close to P_{SAT}. The need to cascade seven stages is mainly due to the very low gain of fifth stage (close to 0 dB). Resistors connected at both gates and drains of the output stage prevent odd mode oscillations. The Doherty-like amplifier has been implemented by a classical topology [16], that includes a Lange coupler at the input to create, between main and peak branches, a delta phase unbalance of 90°. This phase unbalance is then compensated with the quarter-wavelength impedance transformer at the output of the main branch. Regarding the layout of the V-band PA, almost all the matching networks have been designed by using coplanar waveguide with lower ground plane (CPWG). Only the last stage of the Doherty Amplifier has been designed by using classic microstrip (MS) structures at the input and output matching networks. This design strategy has been adopted because, as confirmed by electromagnetic (EM) simulations, passive structures implemented with MS have lower losses compared to CPWG solutions. The four FETs at the output stage are coplanar, so they require a MS-CPWG transition on the gate side while, at the drain side, a CPWG-MS transition is present.

GaN V-band PA implementation and measurements

The seven-stage PA has been manufactured in two separate dies (driver and amplifier) in order to optimize the area in the available reticle, and to reduce the risk in case of performance issues allowing the redesign of the driver or the amplifier independently. A final layout that includes the two circuits into a single MMIC will reduce the uncertainty related to assembly and bondings. The MMIC areas, including pads, are 4.125 mm^2 for the driver and 13.75 mm^2 for the amplifier, respectively. The total power consumption is 16.8 W with the two dies powered on together. Chip photographs are reported in Fig. 5, whereas Figs. 6 and 7 show the full assembly of the MMICs with the passive structures and the test bench. Each DC-pad of the MMICs is connected to a chip capacitor toward ground and then wire-bonded to the printed circuit board (PCB) manufactured on FR4 substrate.

All the gates have a 20 Ω resistor in series on the PCB to suppress oscillations. These resistors do not affect the DC bias point of the stages. No gate current was measured even at high compression level. All measurement results reported in this paper are referred to the test-jig reference plane. The driver input and the Amplifier output are bonded respectively to a 5-mils-thick MS on an internally processed thin-film alumina substrate.

Each MS line on alumina is shaped to work as launcher respectively for input and output MS-waveguide transitions in WR15, as shown in Fig. 6. It is worth to note that, since the MMICs are mounted on a module with WR15 waveguide interface, a low frequency instability cannot be observed on RF output. The amplifier behaves as expected in simulation, and no evidence of instability has been observed. Further, the bias lines on the PCB have filtering capacitors (10 nF and 1 μF) and 47-Ω series resistor, only on gate lines, to minimize the risk of auto-oscillation. The PA covers with reasonable margins the desired 59–71 GHz operating bandwidth and well fits simulation and measurement results, confirming the design robustness also with such a complex assembly structure. The comparison between simulation and measurement results of S_{21} @ 25°C of eight separate PAs is reported in Fig. 8a. The observed spread between the measured samples is ascribed to process variations (in MMICs, alumina MS lines and waveguide transitions) and to the manual assembly of the eight modules (wire

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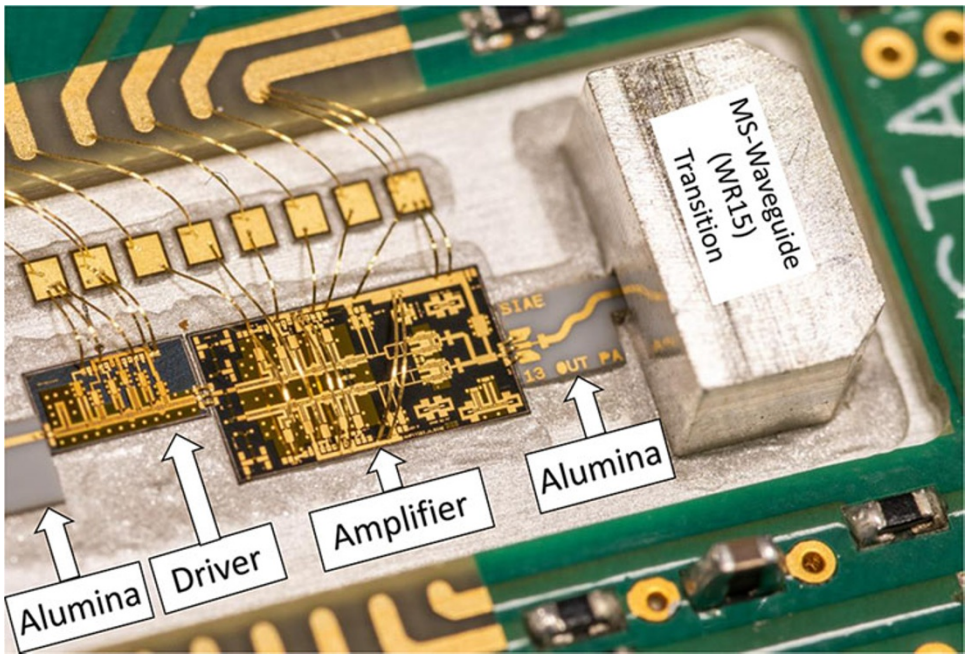

Figure 6. Full assembly of the V-band PA with highlighted GaN MMICs and passive structures.

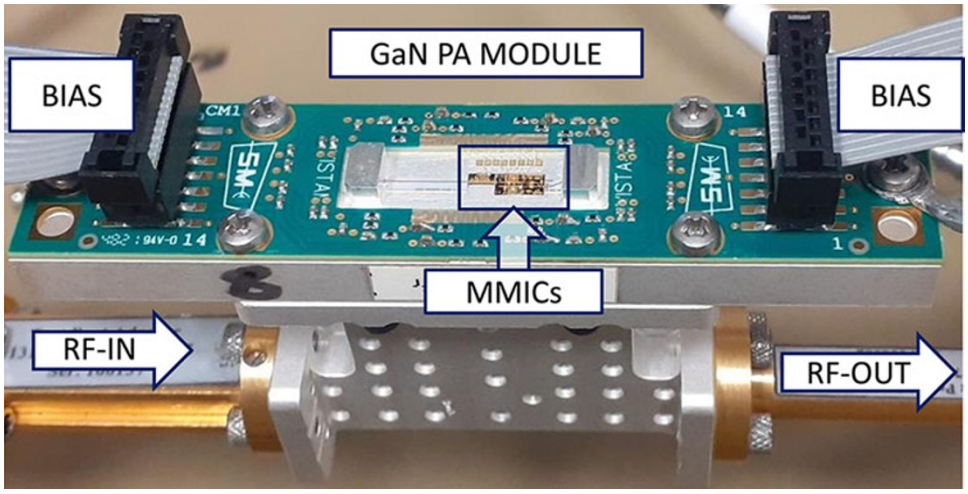

Figure 7. Photo of the full connected V-band GaN PA used in the test bench.

bonding). The maximum $|S_{21}|$ ranges from 26 to 29.5 dB across the eight-characterized PA samples and occurs close to the lower operating band limit. Measurement and simulation results of scattering parameters are shown in Figs. 8 and (input/output MS-waveguide transitions included).

The PA has been measured also by varying the temperature from −25°C to 85°C, and the results are shown in Table 3. Simulation and measurement results of P_{1dB} and PAE @ P_{1dB} are shown in Fig. 10a and b, respectively. All the results confirm that the FET models provided by the foundry are quite accurate for all the FETs biased at 300 mA/mm. A minor discrepancy has however been observed for the two FETs of the fifth stage, those biased in deep AB class. In this case, the current density used in simulation does not produce the expected gain expansion needed to shift the P_{1dB} close to P_{SAT}. This inconsistency was indeed expected, since the FET models provided by the foundry were extracted for class A operation.

However, by reducing the current density of fifth stage, it was possible to further increase the fitting between measurements and simulations results, as shown in Fig. 11 where gain, P_{OUT}, and PAE vs. P_{IN} @65 GHz are shown. An accurate comparison with other works in the literature is very challenging since this work is focused on the performance of a PA biased for space environment (i.e. applying derated voltages) and great attention has been paid to the yield analysis and to the robustness in terms of performance of the entire module assembly. However, a rough comparison can be done with other works summarized in Table 4:

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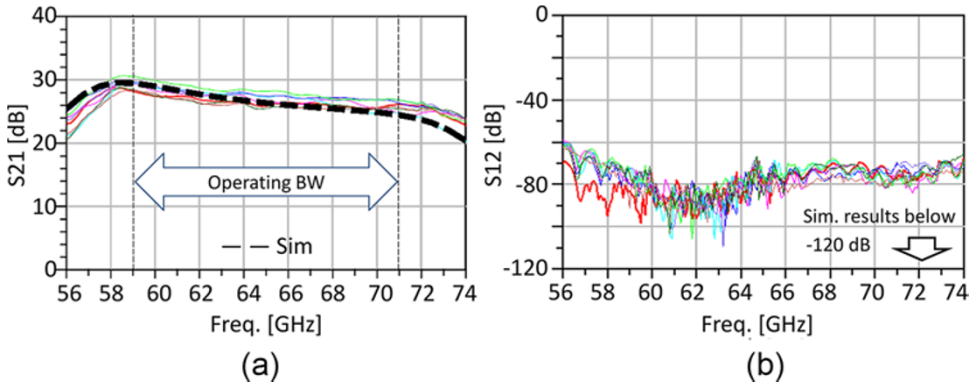

Figure 8. V-band PAs $|S_{21}|$ and $|S_{12}|$: measurements (coloured lines) and simulation (dashed line) results of 8 samples.

Table 3. V-band PAs: Measurements versus temperature

	S21 (dB)[a]			P_{1dB} (dBm)[a]			PAE@P_{1dB} (%)[a]		
Frequency (GHz)	59	65	71	59	65	71	59	65	71
$T_1 = 25°C$	28.8	25.1	24.2	32.8	32.9	31.6	9.0	8.7	7.7
$T_2 = -25°C$	33.5	30.0	29.5	33.1	33.1	31.8	9.1	9.1	7.5
$T_3 = 85°C$	25.0	21.7	20.5	32.6	32.7	31.2	9.2	8.9	7.3

[a]All these values are referred to a specific sample used for the measurements at several temperatures and are used to analyze the performance variation of PA in temperature.

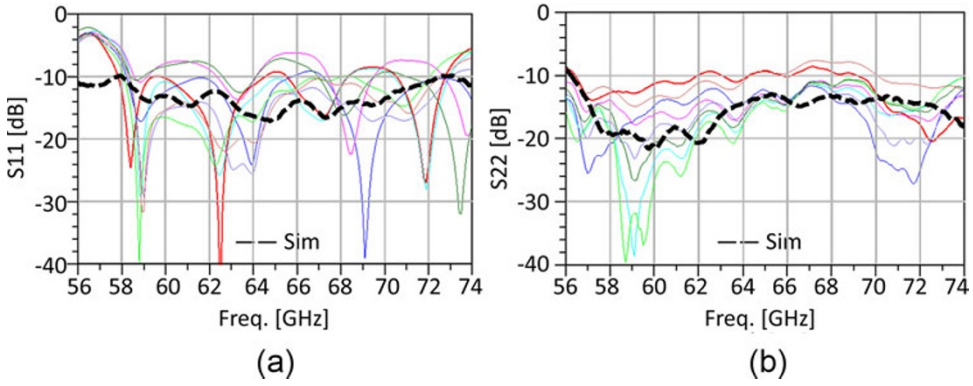

Figure 9. V-band PAs $|S_{11}|$ and $|S_{22}|$: measurements (coloured lines) and simulation (dashed line) results of 8 samples.

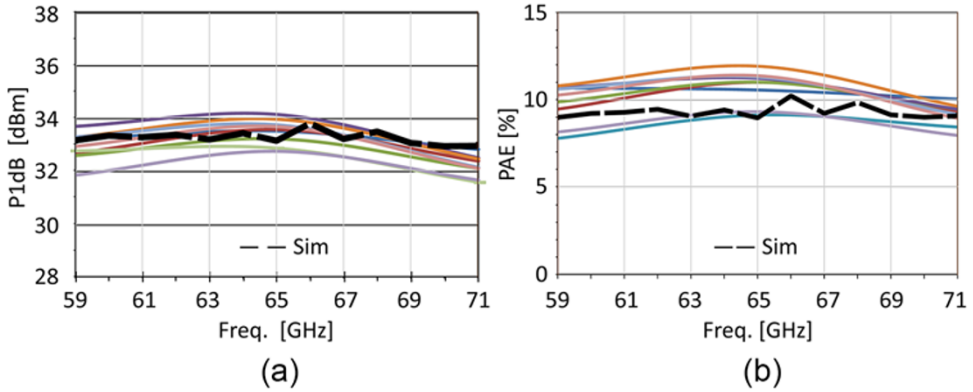

Figure 10. V-band PA: measured (8 samples, coloured lines) and simulated (dashed line) P_{1dB} and PAE @ P_{1dB} at 25°C.

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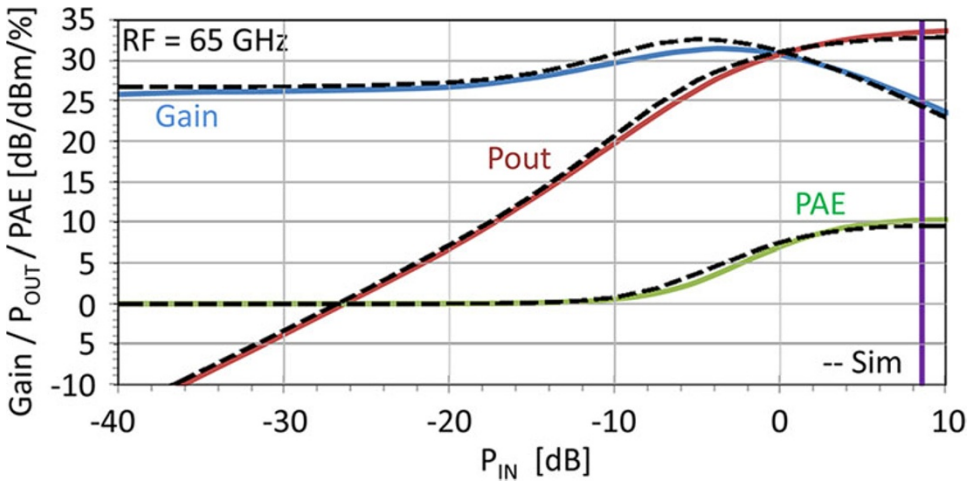

Figure 11. V-band PA: Measured and simulated gain, P_{OUT} and PAE vs. P_{IN} at 65 GHz.

Table 4. V-band power amplifiers: Comparison with the state of the art

Ref.	Tech. process	Freq. (GHz)	$Gain_{MAX}$ (dB)	$Psat_{MAX}$ (dBm)	PAE_{MAX} (%)	Test config.	Year
[12][a]	0.10 μm GaN/SiC HEMT	50–75	30.0	29.3	13.5%	On die	**2018**
[16]	0.10 μm GaN/SiC HEMT	57–61	19.1	36.9	25%	On die	**2021**
[18]	0.10 μm GaN/SiC HEMT	63–73	27	29.6	17%	On die	**2023**
[19]	0.10 μm InAlN/GaN/SiC HEMT	54–60	22	31.0	17%	On die	**2023**
[20][a]	0.15 μm GaN/SiC HEMT	62–72	11.3	31.3	14.7%	On die	**2023**
[21]	0.10 μm GaN/SiC HEMT	74–81	15	36.0	15.3%	On die	**2023**
This work[a]	**0.10 μm GaN/SiC HEMT**	**59–71**	**29.5**	**34.2**	**11.9%**	**Module**	**2023**

[a]Derated V_D

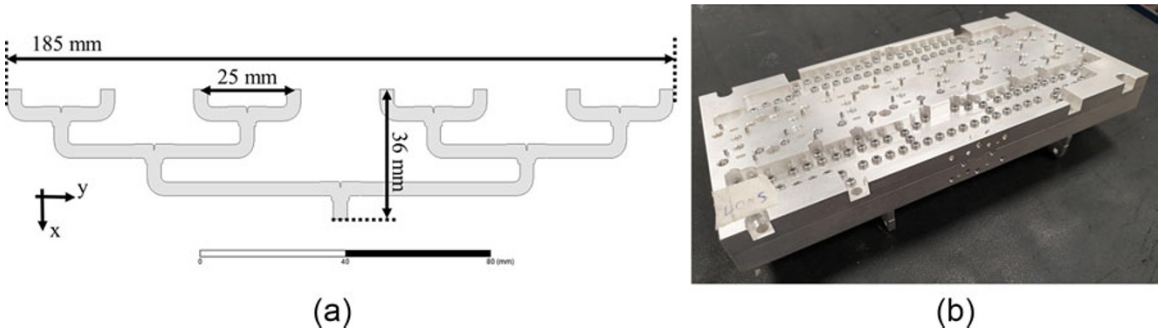

Figure 12. (a) Top view of the designed waveguide tree with the overall dimensions and the pitch between the ports. (b) lateral view of the manufactured waveguide splitter.

Splitter/Combiner development

The design of the power splitter/combiner relies on a standard WR15 metallic hollow waveguide branching with three binary levels of H-plane tees. The choice of avoiding balancing resistors guarantees the best insertion loss and lower manufacturing complexity at the cost of poor isolation between the active chains. However, this behavior does not imply a performance degradation since the splitting block is perfectly symmetric: only manufacturing tolerance contributes to possible phase and amplitude variations. A 3D EM simulator (Ansys Electronics Desktop environment) has been used to perform simulations and final optimizations. The H-plane tee junction and the H- and E-plane 90° bends have been designed and optimized independently and then connected through standard WR15 sections, sketched in Fig. 12a. From a mechanical point of view, the final assembly for the HPA is made by two CNC milled bodies: the bottom one with the planar H-plane waveguide structures while its cover is a thick body which serves as lid for the waveguide and includes WR15 openings for the ports toward the MMICs.

The bodies are made by CNC machined aluminum alloy finished with 3 μm of silver treatment; the mechanical assembly is shown in Fig. 12b. Since this HPA is conceived for space-oriented subsystems, specific attention has been dedicated to save weight. One considered option is to avoid the screw assembly and

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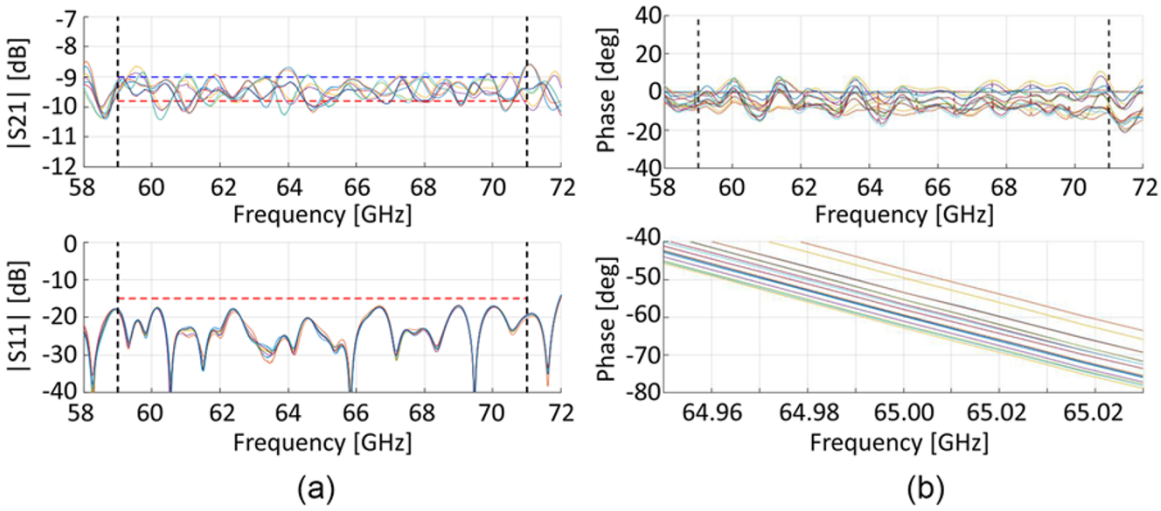

Figure 13. (a) Top: superposition of all the measured transmission parameters; bottom: overlap between all the $|S_{11}|$, measured when each amplifier port was under test with the others terminated on a WR15 waveguide matched load. (b) top: measured phase difference between the first reference channel and all the other waveguide outputs. Bottom: phase measurements of all the chains in the middle of the band (65 GHz) to assess maximum phase unbalance.

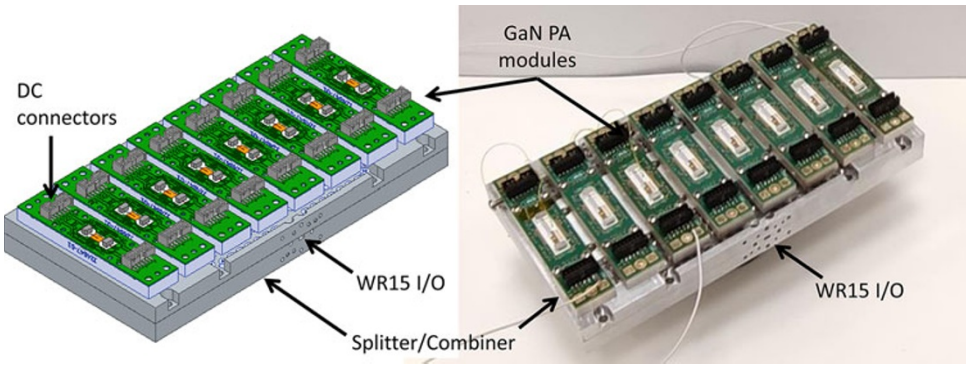

Figure 14. 3D model view and photo of the 10 W GaN HPA.

directly solder the two bodies, since steel screws account themselves for 15% of the overall mass. For prototyping purposes, the PAs are currently glued each to a metal carrier, which provides an easier-to-handle base for bonding and precision assembly of the dies. In future perspective, carriers can be avoided, and the active circuits will be mounted directly on the lid of the combiner. This step ahead will save weight and ease the thermal dissipation.

The scattering parameters have been measured by means of a Rohde & Schwarz ZVA50 vector network analyzer, combined with two ZVA-Z75 frequency extenders.

Figure 13a shows the magnitude of S-parameters of the passive division/recombination network. All the waveguide routings have shown a matching better than 15 dB, even with some margin outside the intended frequency spectrum. Moreover, the average mean insertion loss is approximately 0.6 dB (plus 9 dB intrinsically given by the three levels of tee junctions), and the ripple superposed to the transmission parameter is limited within 1 dB.

Finally, the behavior of phase versus frequency behavior is reported in Fig. 13b. Phase coherence between the paths is crucial for the parallelization of PAs. In fact, phase unbalances directly lead to recombination losses with penalty in the overall HPA gain and maximum output power. The picture shows the wideband phase difference between the first reference channel and all the other waveguide outputs. Additionally, an enlarged view focused on the middle of the band (65 GHz) highlights the maximum phase deviation between paths, which is limited to 15°. This value leads in the worst case a gain penalty of less than 0.05 dB in the overall HPA.

Experimental results

The 10-W GaN HPA has been realized assembling eight of the GaN PA modules described in the "GaN V-band MMIC: Design and measurements" section, each one tested stand alone, with the waveguide splitter/combiner developed as discussed in the "Splitter/Combiner development" section. Figure 14 provides a 3D view and a photograph of the HPA. The overall weight of the HPA module is 770 g, without specific weight-saving solutions implemented yet.

An internally developed bias board controlled by a dedicated graphical user interface software has been used to control all the voltages.

Particular attention has been dedicated to the connection of the ground and drain lines by choosing a wire diameter and interconnection topology able to carry up to 15 A with minimum voltage drop. The HPA temperature has been monitored by using PTC thermistors mounted near the MMICs. During the measurement sessions, at thermal equilibrium, the measured temperature was close to 40°C.

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The biasing of the whole HPA has been achieved by tuning the bias of each of the eight modules individually to maximize the output P_{1dB}. Once all the modules are powered together with a drain voltage of 11.25 V, the total absorbed DC current is 12 A (1.5 A for each PA module).

The test-bench used to characterize the HPA is shown in Fig. 15, where the number of connections stand as evidence of the complexity of the component, involving 32 separate bias voltages and several control components.

The small-signal gain is greater than 22 dB (considering a total loss for I/O waveguide splitter/combiner of 2 dB) over the whole operating bandwidth with a maximum of 25.5 dB at 59 GHz, as shown in Fig. 16. The target frequency bandwidth is fully covered with some margin at both upper and lower bounds. Input and output matching is also better than 10 dB within the target bandwidth.

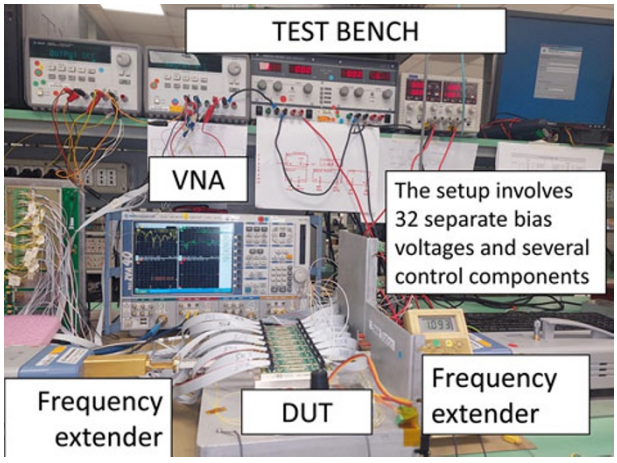

Figure 15. 10 W GaN HPA: Test bench.

Regarding large signal tests, the biasing of all the modules has been maintained at the same values used for S-parameters, i.e. $V_D = 11.25$ V and a total quiescent current (I_D) of 12 A. A P_{1dB} higher than 39.4 dBm over all the operating frequency band with a maximum of 40.3 dBm has been measured. The saturated power (P_{SAT}) is higher than 39.6 dBm over all the operating frequency band with a maximum of 40.6 dBm. P_{1dB} is close to P_{SAT} by about 0.5 dB as shown in Fig. 16.

These measurement results confirm the simulated ones since the gain expansion created with stage 5 has increased the P_{1dB} to a value close to the saturated power. Another important parameter considered during the measurement campaign has been the PAE. PAE has been evaluated at P_{1dB} and it is in the range between 6.2% and 6.5%.

It is worth to note that, all presented results are obtained in continuous wave (CW) conditions. Fan is used to cool the device under test (DUT), its temperature is monitored using thermistors. All measurements are taken when thermal equilibrium is reached.

Table 5 summarizes the measured performances and the key features of the GaN HPA.

Further tests have been carried out with modulated signals to evaluate the HPA's linearity. Maximum powers levels at the

Table 5. 10-W GaN HPA: Performance summary

10-W GaN HPA key features		Frequency (GHz)	59	65	71
Technology process	GaN 100-nm	Gain (dB)	25.6	23.4	22.1
RF IN/OUT connection	WR–15	P_{1dB} (dBm)	40.3	40.3	39.4
n° of parallelized PA	8	P_{SAT} (dBm)	40.6	40.5	39.6
Power consumption (W)	180	PAE@P_{1dB} (%)	6.5	6.2	6.5

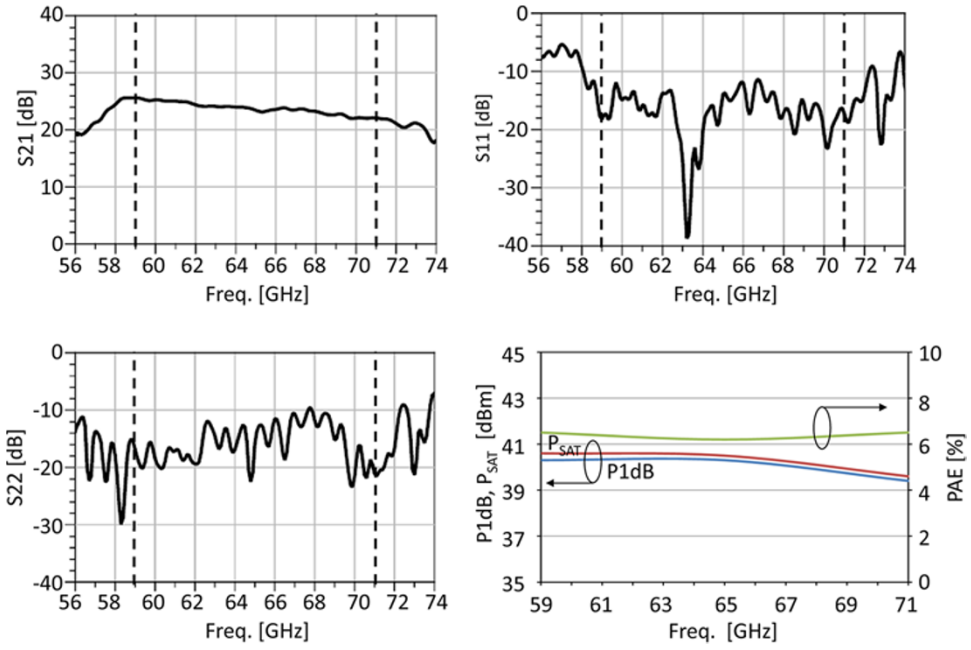

Figure 16. Linear and non-linear measurement results for V-band GaN HPA with bias: $V_D = 11.25$ V, $I_D = 12$ A.

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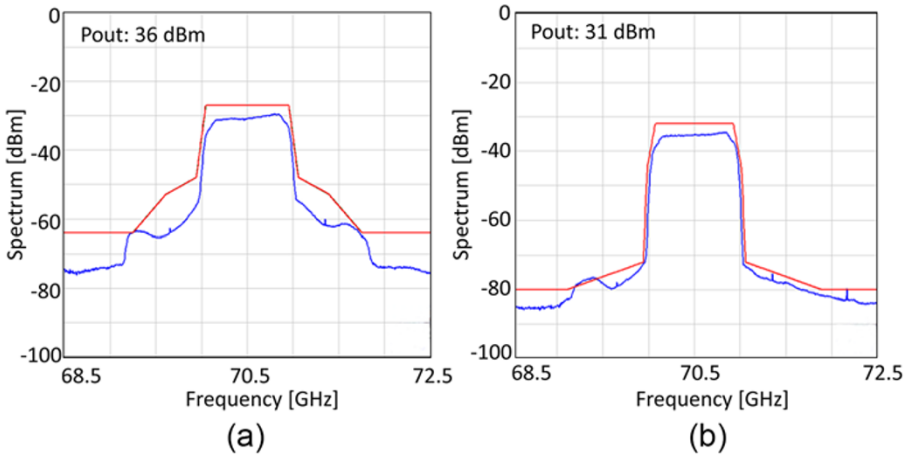

Figure 17. Measured output spectrum (blue) and ETSI mask (red). Test signal used is 4 QAM with 1-GHz channel bandwidth (a) and 256 QAM with 1-GHz channel bandwidth (b).

output of the HPA, compliant with ETSI emission mask [17], of 36 dBm for 4-QAM with 1-GHz channel bandwidth and 31 dBm for 256-QAM signal with 1-GHz channel bandwidth have been measured. A standard digital polynomial predistortion technique has been leveraged in the transmitter, whose predistortion coefficients have been manually adjusted to partially compensate the nonlinear behavior of the HPA. The use of this predistortion provides the result shown in Fig. 17, complying with ETSI emission masks.

Conclusions

This manuscript demonstrates a V-band 10 W GaN-based HPA suitable as final transmitter stage of a V-band ISL. The proposed structure relies on the parallelization of state-of-the-art GaN-on-SiC PAs branched together by a waveguide combiner, which serves also as mechanical support and I/O interface. The paper reports the design of all the involved building blocks in the HPA assembly and the measurement results in the whole 59–71 GHz operating bandwidth. The entire structure features 25.6 dB of small-signal gain, 40.6 dBm of P_{SAT}, and 6.5% of PAE with a maximum power consumption of 180 W. The first prototype exhibits an unoptimized weight of 770 g, whereas studies already conducted highlight the possibility to match a half-kilogram weight target. The achieved performances have been proved in a controlled environment, but future developments intend to prove the HPA readiness for the real use-case.

Funding statement. This work was funded by ESA through ARTES AT program (4000132546/20/NL/MM).

Author contributions. This declaration remarks that all the authors contributed equally during the work described in the submitted manuscript and in the writing phase of the paper. Each author has specific skills which have been individually exploited to achieve the final goal and the composition of the manuscript. Please, see here below the detailed contribution from each author:

Mr. Giuseppe Sivverini, Mr. Andrea Meazza, Prof. Matteo Oldoni, Mr. Antonio Traversa, and Dr. Alessandro Fonte (listed as corresponding author) had in charge the analysis of the use-case and they worked on the definition of the specification following the requirements from ESA. Dr. Alessandro Fonte also drafted the preliminary form of the manuscript. Mr. Giuseppe Sivverini and Mr. Andrea Meazza designed the GaN V-band MMICs (power amplifier and the amplifier). Dr. Friesicke Christian contributed to provide information on the GaN technology and took preliminary on-wafer measurements of the MMICs. Dr. Stefano Moscato and Dr. Steven Caicedo Mejillones performed the full-wave simulations of the V-band splitter/combiner and took into account the measurements of the realized passive circuits. Mr. Alberto Colzani contributed to the main section of the characterization of the V-band PA mounted on metal carrier and the full high-power-amplifier. Moreover, all authors contributed equally to analyzing data and reaching conclusions, in writing the paper, and in the finalization of the manuscript for each submission steps.

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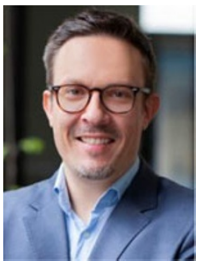

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